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Power-Estimation for On-Chip VLSI Distributed RLC Global Interconnect Using Model Order Reduction Technique

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ABSTRACT

Power is increasingly becoming the bottleneck for the design of high performance VLSI circuits. It is essential to analyze how the various components of power are likely to scale in the future, thereby identifying the key problematic areas. While most analysis focus on the timing aspects of interconnects, power consumption is also important. In this paper, the power distribution estimation of interconnects is studied using a reduced-order model [1]. The relation between power consumption and the poles and residues of a transfer function is derived, and an appropriate driver model is developed, allowing power consumption to be computed efficiently.