

8-Bit Sub Threshold Ripple Carry Adders in 32nm CMOS Technology for Wireless Sensor nodes.

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ABSTRACT

Subthreshold design has been proposed in the literature as an effective technique for designing signal processing circuits needed in wireless sensor nodes powered by sources with limited energy. The full adder cell forms the basic building block of majority of these signal processing circuits. In this paper, 8-Bit subthreshold Ripple Carry Adders (RCAs) for wireless sensor nodes optimized for ultra low power operation are proposed. Major contribution of this work is conversion of BSIM4, Predictive Technology Model (32nm) to EKV model (charge based model). The 8-bit RCAs are simulated with HSPICE (Level =55) using the 32nm CMOS technology at supply voltages ranging from 0.25V to 0.4V. Various metrics such as delay, average power and power delay product (PDP) are simulated and reported for effective twelve different topologies. The circuit designers can choose the full adder topology and the supply voltage that is suitable for their applications. Usage of EKV models results in 11% reduction in power than that of using BSIM models for the adder cell “CB” with supply voltage of 0.2V.

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