Abstract

Historically, most Printed Circuit Board (PCB) testing was done using bed-of-nail in-circuit test equipment. The progress in the field of miniaturization and integration density has possible to design very complex PCBs, which presents very high testability requirements. Boundary scan is now the most promising technology for testing high complexity PCBs. This paper presents scan-based test access port standard for testing complex ICs and also presents a method which allow the extraction of fine-grained timing information using Test Access Port (TAP).

Reference

[3] Mark Horowitz, Andy Chan, Joe Cobrunson, Jim Gasbarro, Thomas Lee, Wing Leung,


Index Terms

Electronics 
Testing

Key words
Printed Circuit Board (PCB)
Test Access Port (TAP)