Design of 0.13um CMOS Two Stage Low Noise Amplifier

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Abstract

A Low Noise amplifier is one of the most commonly used components in analog and digital circuit designs. Low voltage and low power Low Noise amplifier design has become an increasingly interesting subject as many applications switch to portable battery powered operations. An electronic amplifier is an electronic device that increases the power of a signal. This design techniques is needed to allow amplifiers to maintain an acceptable level of performance when the supply voltages are decreased is immense for maintain low noise with high gain. The low-noise amplifier is a special type of electronic amplifier used to amplify very weak signals captured by an antenna. This paper presents a technique for substantially reducing the noise of a CMOS low noise amplifier implemented in the cascade inductive source degeneration topology. This 2.4 GHz Two Stage CMOS 130nm RF Low Noise Amplifier is optimize for low noise at low current with very low power consumption. In this proposed design work the two stage cascade low noise amplifier is used to achieve noise 28 dB, input return loss of >10 and output return loss of > -10 at 1.3 supply voltage.
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References

- Thi Thu Nga Tran, Chim Chye Boon, Manh Anh Do, and Kiat Seng Yeo. A 2.4 GHz ultra low-power high gain LNA utilizing x-match and capacitive feedback input network. 978-1-61284-857-0/11 ©2011 IEEE.
- Hong-Sun Kim, Xiaopeng Li, and Mohammed Ismail. Fellow IEEE A 2.4GHz CMOS Low Noise Amplifier using an Inter-stage Matching Inductor 0-7803-5491-5/99/$10.00 ©2001 IEEE.
- A. Pascht, Member, IEEE. J. Fischer and M. Berroth, Member, IEEE A CMOS Low Noise Amplifier at 2.4 GHz with Active Inductor Load 0-7803-7129-1/01/$10.00 ©2001 IEEE.
- Meng Zhang 1, 2, 3, Zhiqun Li 1, 2, 3 A 2.4 GHz Low Power Common-Gate Low Noise Amplifier for Wireless Sensor Network Applications 978-1-61284-307-0/11 ©2011 IEEE.
- François Belmas1, Frédéric Hameau1, Jean-Michel Fournier2 A 1. 3mW 20dB Gain Low Power Inductorless LNA with 4dB Noise Figure for 2.45GHz ISM Band 978-1-4244-8292-4/11 ©2011 IEEE.
- Sambit Datta*, Kunal Datta*, Ashudeb Dutta#, Tarun Kanti Bhattacharyya* A Concurrent Low-Area Dual Band 0.9/2.4 GHz LNA in 0.13?m RF CMOS Technology for Multi-Band Wireless Receiver 978-1-4244-7456-1/10 ©2010 IEEE.

Index Terms

Computer Science
Circuits And Systems
Keywords
CMOS  two stage  cascode low noise amplifier  noise  gain and power.