Abstract

In this paper, we are implementing the Convolutional encoder and viterbi decoder with code rate 2/3 using verilog. The main issue of this paper is to implement the RTL level model of Convolutional encoder and viterbi decoder, with the testing results of behavior model. We tried to achieve a low silicon cost. The viterbi algorithm, used for Convolutional codes extensively employed decoding algorithm for Convolutional codes. This paper is realized using verilog HDL. It is simulated and synthesized using Modelsim Altera 10.1d.
Simulation of Convolutional Encoder and Viterbi Decoder using Verilog

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Index Terms

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