Abstract

In this paper, we are implementing the Convolutional encoder and viterbi decoder with code rate 2/3 using verilog. The main issue of this paper is to implement the RTL level model of Convolutional encoder and viterbi decoder, with the testing results of behavior model. We tried to achieve a low silicon cost. The viterbi algorithm, used for Convolutional codes extensively employed decoding algorithm for Convolutional codes. This paper is realized using verilog HDL. It is simulated and synthesized using Modelsim Altera 10.1d.

References

- Simon Haykin and Michael Moher: Modern wireless communications; Pearson Prentice Hall, 2005
- Simon Haykin; Digital communications; Wiley, cop. 1988
- Samir Palnitkar: Verilog HDL a Guide to Digital Design and Synthesis; sun soft press (1996);
- Chip Fleming: A Tutorial on Convolutional Coding with Viterbi Decoding; Spectrum Application; Jun, 2003;
- Pravalli. kolakaluri, R. Suryaprakash: HDL Implementation of Convolutional encoder and viterbi decoder; July, 2012;
- Rohan M. Pednekar, Dayanand B M: Design and Implementation of Convolutional encoder and viterbi decoder; 2013;
- Swati Gupta, Rajesh Mehra: FPGA Implementation of viterbi decoder using track back architecture; June, 2011;
- Mahe Jabeen, Salma Khan: Design of Convolutional encoder and Reconfigurable viterbi decoder; (sept 2012)

Index Terms

Computer Science

Circuits And Systems

Keywords

Convolutional encoder  viterbi decoder  Modelism10. 1d  viterbi algorithm  trellis diagram

simulation.