Abstract

Fault Tolerant reversible decoders are the prerequisite of high performance computing systems. In this paper, an optimized reversible fault tolerant decoder has been proposed by using novel cost effective gates named Reversible Fault Tolerant Decoder (RDC) and Double Fredkin Gate (DFG). Several lower bounds on the numbers of gates, garbage and quantum costs are also proposed to generalize the architecture of n-to-2n reversible decoder. The comparative performance analysis shows that the proposed design outperforms the existing designs in terms of number of gates used, quantum cost, delay, ancilla inputs and design complexity.

References

Reversible Decoder Using MOS Transistor. 26th International Conference on VLSI Design. 368-373. India.


Index Terms

Computer Science
Circuits And Systems

Keywords