Abstract

Bio-Implantable Microsystems such as the cardiac pacemaker, retinal and neural implant provides substitute for a missing biological part, support an impaired biological structure or even upgrade the existing biological system. These Microsystems require ultra-low power miniature integrated circuit technology for long term reliable operation. For energy constraint applications like the implantable devices, the performance requirement are secondary factors while energy efficiency, low power, high density and high robustness are of primary concern. For low power operation, scaling the supply voltage into sub-threshold region is possible and is an effective technique for power reduction. Implantable devices require minimum energy consumption and prolonged battery lifetime. So these systems demand low leakage currents without sacrificing much on performance. In this work a new 9T MTIP3 SRAM Bit-Cell is proposed at 45nm
CMOS technology using multi-threshold (MTCMOS) design technique. The static power saving in MTIP3 is 99.83% as compared to conventional 6T and 23.82% as compared to IP3 at VDD=0.8V. The dynamic power saving of read1 in MTIP3 is 86.37% as compared to 6T. The dynamic power saving of write1 in MTIP3 is 66.23% as compared to IP3. The access time of MTIP3 is 16.94% less than 6T. The energy saving during hold mode in MTIP3 is 99.5% as compared to 6T. Static Noise Margins are improved by 2.07% compared to IP3 at VDD=0.7V.

References


Index Terms

Computer Science  Information Science

Keywords
6T SRAM  Bio-Implants  Microsystems  MTIP3 SRAM  Sub-threshold Region
Voltage Scaling.