Abstract

This paper addresses the problem of application mapping onto Butterfly-Fat-Tree (BFT) based Network-on-Chip design. It proposes a new mapping technique based on discrete Particle Swarm Optimization (PSO) to map the cores of the core graph to the routers. The basic PSO has been augmented by running multiple PSO and deterministically generating a part of the initial population for PSO. The mapping results have been compared with well-known techniques reported in the literature for a number of benchmark applications. The reported strategy produces results superior to those obtained via existing approaches within a reasonable CPU time.

References

- W. J. Dally, B. Towles, "Route Packets, Not Wires: On-Chip Interconnection


- L. Benini, &quot;Application Specific NoC Design,&quot; IEEE Design, Automation and Test in Europe Conference (DATE'06), vol. 1, pp. 1–5, 2006.


- M. Janidarmian, A. Khademzadeh, M. Tavanpour, &quot;Onyx: A New Heuristic
Application Mapping onto Butterfly-Fat-Tree based Network-on-Chip using Discrete Particle Swarm Optimization


Index Terms

Computer Science    Networks

Keywords

Application mapping    Network-on-Chip    System-on-Chip    Butterfly-Fat-Tree
Discrete Particle Swarm Optimization