Abstract

Three-dimensional Network-On-Chips (3D NOC) are the most efficient communication structures for complex multi-processor System-On-Chips (SOC). Such structures utilize short vertical interconnects in 3D ICs together with scalability of NOC to improve performance of communications in SOCs. By scaling trends in 3D integration, probability of fault occurrence increases that leads to low yield of links, especially TSV-based vertical links in 3D NOCs. In this paper, FT-Z-OE (Fault Tolerant Z Odd-Even) routing, a distributed routing to tolerate permanent faults on vertical links of 3D NOCs is proposed. FT-Z-OE is designed to have low overhead because of no need to any routing table or global information of faults in the network. The proposed routing is evaluated using a cycle-accurate network simulator and compared to planar-adaptive routing for a 3D mesh-based network. It is shown that FT-Z-OE significantly outperforms planar-adaptive in the terms of latency and throughput under synthetic traffic patterns.

References

- Dally, W. J. and Towles, B., 2001, Route packets, not wires: on-chip interconnection
FT-Z-OE: A Fault Tolerant and Low Overhead Routing Algorithm on TSV-based 3D Network on Chip Links

- Benini, L. and De Micheli, L. , 2002, Networks on chips: a new SoC paradigm, Computer 35 (1), pp. 70-78.
FT-Z-OE: A Fault Tolerant and Low Overhead Routing Algorithm on TSV-based 3D Network on Chip Links

- https://noc.s.stanford.edu/

Index Terms

Computer Science Networks

Keywords