Abstract

Ternary content-addressable memory (TCAM) is often used in high speed search intensive applications such as ATM switch, IP filters. Hence, currently ZTCAM, is introduced which emulates the TCAM functionality with SRAM. It has some drawbacks such as low scalability, low storage density, slow access time and high cost. But this paper proposes novel memory architecture of existing Z-TCAM, but with STTRAM instead of SRAM. Hence the area, delay and power by using lower power consumption Spin Transfer Torque RAM (STT RAM) instead of SRAM. The detailed implementation results and power measurements for each design have been reported thoroughly.

References

A Low Power VLSI Implementation of STTRAM based TCAM for High Speed Switching Circuits

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**Index Terms**

Computer Science Programming Language

**Keywords**

Ternary Content Addressable Memory Spin Transfer Torque RAM Hybrid Partitioning.