Abstract

The implementation of residue number system reverse converters based on well-known regular and modular parallel prefix adders is analyzed. The VLSI implementation results show a significant delay reduction and area × time² improvements, all this at the cost of higher power consumption, which is the main reason preventing the use of parallel-prefix adders to achieve high-speed reverse converters in recent systems. Hence, to solve the high power consumption problem, novel specific hybrid parallel-prefix based adder components that provide better trade-off between delay and power consumption are herein presented to design reverse converters. We propose Parallel distributed arithmetic convolution technique in Reverse Converter to increase the system performance.

References

Design and Implementation of RNS Reverse Converter using Parallel Prefix Adders


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Design and Implementation of RNS Reverse Converter using Parallel Prefix Adders


Index Terms

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Keywords

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