Abstract

The popularity and necessity of portable electronic systems by users have strongly influenced VLSI designers to make great effort for reduced silicon area, improved speeds, long duration battery life, and great reliability. The VLSI designers always try to save power consumption while designing a system. In this paper, an efficient methodology is presented to improve the output swing level of GDI gates. New designs of GDI based basic digital (AND, OR, XOR, XNOR) gates are presented using single pass transistors to improve swing level of GDI gates. The new design of basic gates with combination of GDI logic and pass transistor logic is called hybrid GDI technique. Compared to existing GDI technique with buffer restoration circuits, hybrid GDI implementation provides full swing output voltage in all digital circuits. Also it shows less power and less delay with about 60% area increase as compared to basic GDI.

References


- Ashouei, M., Singh, A. D. and Chatterjee, A., "Reconfiguring CMOS as Pseudo N/PMOS for Defect Tolerance in Nano-Scale CMOS," IEEE International Conference on
Low Power 10T XOR based 1 Bit Full Adder


Index Terms

Computer Science

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Keywords

GDI  Full Adder  XOR  XNOR  Low power