Abstract

LDPC codes provide good random error performance nearer to Shannon limit. The LDPC codes have some residue errors which cannot be corrected even after large number of iterations such errors can be corrected by concatenating LDPC codes with RS codes. This paper describes the development of an iterative decoder scheme for LDPC-RS product codes which made LDPC codes and Turbo codes popular. The iterative structure consists of a soft decision decoding of LDPC codes and hard decision decoding of RS codes. The concatenated scheme provides higher performance than the iterative decoder for LDPC codes. The iterative scheme is developed in MATLAB and FPGA kit is used for practical verification.

References

- D. J. C. MacKay and R. M. Neal, "Near Shannon limit performance of low
Development and Verification of Iterative Decoder for LDPC-RS Product Codes

Index Terms

Computer Science
Software Engineering

Keywords
LDPC-RS SVM EE Log-SP SSD BMA Product codes Iterative decoder