Abstract

Three dimensional Networks-on-Chip (3D NoCs) have attracted a growing interest to solve on-chip communication demands of future multi-core embedded systems. However, 3D NoCs have not been completely accepted into the mainstream due to issues such as the high cost and complexity of manufacturing 3D vertical wires, larger memory, area and power consumption of 3D NoC components than that of conventional 2D NoC. This paper presents a brief about 3D NoCs optimization techniques with focus on modeling and evaluation of alternate NoC topologies, routing algorithms and mapping techniques to achieve optimized area, power and performance parameters (latency and throughput). Particularly, we investigate novel 3D NoC router architectures and their possible combinations which aim at achieving lower area and power consumption of on-chip communication components with a minimal performance trade-off.

References

A Study of Optimization Techniques for 3D Networks-on-Chip Architectures for Low Power and High Performance Applications


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