Compact, High Speed and Low power Decoders for Future Generation System Building

Abstract

Electronic system building has become highly competitive from the point of reducing area, power and increasing the speed. To address these issues, many technologies are being tried. Quantum Dot Cellular Automation is one such technology. This technology is in its infant state as far as its physical implementation and verification are concerned. However the researchers have come out with theoretical models and proposed many compact, fast and low power dissipating digital blocks. Decoders are one of the standard combinational modules used as the basic building blocks for efficient digital system design. Here in this paper we implement decoders in QCA using different techniques and analyze them with respect to area, time and energy. From the implementation and simulation results obtained using QCADESIGNER version 2.0.3 we have observed that, the 2:4 decoders implemented with and without the enable input using both single layer and multilayer techniques utilize minimum area, time and energy.


**Index Terms**

Computer Science  
Circuits and Systems

**Keywords**

Quantum Dot Cellular Automata (QCA), Decoder, Coincident Decoding, Tree Decoding, Universal Module.