Implementation for Minimization of Computation Time of Partial Products for Designing Multipliers using Tabulated Vedic Mathematics

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Abstract

Multiplication is the most time consuming process in various signal processing operations like Convolution, Circular Convolution, auto-correlation, and Cross Correlation, Image processing applications such as edge detection, microprocessors arithmetic and logical units etc. The multiplier circuit uses adder logic which reduces speed of operation due to its path propagation delay. The designs used offer tradeoffs between Computational time area, latency and throughput for performing multiplication. In this paper an ancient Indian Vedic mathematics sutras base multiplier have been proposed with Urddha Tiryakbhyam sutra. In this methodology the length of input sequence used for multiplication varies from two to eight.

References


**Index Terms**

Computer Science  Applied Mathematics

**Keywords**

Multiplier circuit