Abstract

This paper presents the effect of negative bias temperature instability (NBTI) on a 6T CMOS SRAM cell and a technique to correct the NBTI induced error. The effect of NBTI on the generation of interface traps and Ids-Vgs characteristics is analyzed. The degradation of static noise margin and PMOS transistor's Vth with increase in simulation time is analyzed in SRAM cell. Threshold voltage degradation is simulated at two different technologies and it is found that NBTI degradation is prominent in lower technology nodes. As memories occupy the maximum area on a chip, thus, more robust SRAM design is required for high reliability of SRAM cell. MOSFET reliability analysis (MOSRA) model is used to simulate the effects of Bias Temperature Instability and hot carrier injection. Error introduced because of NBTI is corrected using a bit flipping technique.

References


Index Terms
Computer Science  
Circuits and Systems
Impact of Negative Bias Temperature Instability on 6T CMOS SRAM Cell Performance

Keywords

Negative Bias Temperature Instability (NBTI), Static Noise Margin (SNM), SRAM, CMOS, MOSFET.