Abstract

Reversible rationale is all that much sought after for the future figuring advancements as they are known not low power dissemination having its applications in Low Power CMOS, Quantum Computing, Nanotechnology, and picture preparing. Adders and multipliers are fundamental building blocks in many computational units. In this paper we have presented and implemented irreversible and reversible Baugh Wooley approach using standard irreversible and reversible logic gates/cells. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. It is proved that the proposed multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, constant inputs, garbage outputs and number of transistors required.

References

1. H. Thapliyal and N. Ranganathan, "Design of Efficient Reversible Binary Subtractors Based oNew Reversible Gate," Proc. of the I Computer Society Annual Symposium on VLSI,
2009.

Index Terms

Computer Science

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Keywords

Irreversible Multiplier, Baugh Wooley Approach, Reversible Multiplier, Garbage Output, Quantum Cost