Abstract

Full Adder is a fundamental element that is used in all the processor for not only in ALU but in various part of the chipset. The work proposes a Hybrid design methodology to contribute the requirements for the designing of full adder with reduced delay. The Analysis of the designed full adder is done at 270C and 700C temperature range in CMOS 120 nm, 90 nm, and 50 nm technologies using Microwind tool. The result shows the comparison between different CMOS technologies in terms of delay and power dissipation. A comparison is also done in terms of delay of the designed adder with previously known adder cells, which shows the advantage of the proposed design.

References


Index Terms

Computer Science Circuits and Systems

Keywords

Full Adder, Hybrid design, Transmission gate (TG), CMOS technologies, pass transistor logic (PTL), power delay product (PDP), arithmetic and logic unit (ALU).