Abstract

Fast Fourier Transform (FFT) being the most important block in many signal processing and communication systems, consumes more power due to its huge computational complexity. Hence, low power design for FFT hardware gains the focus of researchers now-a-days. There are many algorithms and architectures proposed in the literature to achieve lower computational complexity and power dissipation. In this work, some of the best suitable algorithms and architectures for hardware implementation are analyzed in terms of complexity, speed and power consumption by using Xilinx ISE tools and proposed a low power and high performance architecture and algorithm combination for FFT computations.

References

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Index Terms

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Keywords

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