Abstract

Single Electron Transistor (SET) is an advanced technology for future low power VLSI devices. SET has high integration density and a low power consumption device. While building logic circuits that comprise only of SETs, it is observed that the gate voltage at the input must be higher than the power supply of SET for better switching characteristics. This limitation of SET in the power and gate supply voltages makes it practically inappropriate to build circuits. An approach to overcome this problem, hybridization of SET and CMOS transistor is implemented. In this paper, different types of hybrid SET-MOS circuits are designed such as inverter and NAND gate and by using above two circuits, 2:4 hybrid SET-MOS decoder is designed and implemented. All the circuits are verified by means of PSpice simulation software version 16.5.

References


**Index Terms**

| Computer Science | Circuits and Systems |
Keywords

Single Electron Transistor (SET), CMOS, Coulomb Blockade, Orthodox Theory, Hybrid SET-MOS, Decoder, Pspice