Abstract

Continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits. Low power consumption and smaller area are the most important criteria for the fabrication of DSP systems. Static random access memories (SRAMs) consist of almost 90% of very large scale integrated (VLSI) circuits. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development toward more compact design rules and, consequently, toward higher storage densities. This paper deals with design of low power static random-access memory (RAM) cells and peripheral circuits for standalone RAMs, in 32nm focusing on stable operation and reduced leakage power dissipation. The work is carried out on Tanner Tool version 13 at 32nm technology.

References

Comparative Analysis of Low Leakage SRAM Cell at 32nm Technology


19. Yen-Jen Chang, Feipei Lai and Chia-Lin Yang, "Zero-aware asymmetric SRAM cell for...


**Index Terms**

Computer Science
Circuits and Systems

**Keywords**