Abstract

Digital multipliers are most widely used component in applications such as convolution, Fourier transform, discrete cosine transforms, and digital filtering. Because outturn of these applications mainly depends on multiplier speed, therefore multipliers must be designed efficiently. In the proposed architecture, a variable-latency multiplier design with novel AHL architecture and a razor flip flop is used, which results in reduced delay and increased speed than the existing system. Meanwhile proposed architecture is used to compare array multiplier, column-bypassing multiplier, row-bypassing multiplier and Vedic multiplier. The experimental result shows that the Vedic multiplier has better performance in power consumption and delay. Here in this work Vedic multiplication is done using Urdhva Tiryakbhyam Sutra (Algorithm), which results in minimum delay. Thus using Vedic multiplier ALU is designed which results in enhanced performance compared to contemporary design.

**Index Terms**

Computer Science  
Circuits and Systems

**Keywords**

Adaptive hold logic (AHL), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), variable latency, Vedic mathematics, Urdhva-Tiryakhyam sutra
(Algorithm).