Abstract

This paper presents a differential architecture of CMOS transimpedance amplifier designed to obtain an input capacitive load insensitive and a very low noise structure. The proposed TIA is dependent on the differential structure and consists of a regulated cascode block and a differential amplifier along with active feedback. To increase the bandwidth of the amplifier, series inductive peaking and a capacitive degeneration step are employed. Simulation results show that the TIA achieves 100 GHz bandwidth, 80.4 dBΩ transimpedance gain, and 20 pA/noise.

References

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2010.
5. Danddan Chen, Kiat Seng Yeo, Senior Member, IEEE, Xiaomeng Shi, Manh Anh Do, Senior Member, IEEE Chirn Chye Boon Senior Member, IEEE, and Wei Meng Lim, “Cross-Coupled Current Conveyor Based CMOS Transimpedance Amplifier for Broadband Data Transmission” IEEE transactions on very large scale integration (vlsi) systems, vol. 21, no. 8, august 2013.
15. Omeed Momeni, Student Member, IEEE, Hossein Hashemi, Member, IEEE, and Ehsan Afshari, Member, IEEE A 10-Gb/s Inductorless Transimpedance Amplifier IEEE transactions on circuits and systems—II: express briefs, vol. 57, no. 12, december 2010
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Index Terms

Computer Science                  Circuits and Systems

Keywords

CMOS, Inductive series peaking, Transimpedance amplifier (TIA), Bandwidth enhancement, RGC, Capacitive degeneration, Active feedback.