Abstract

This paper presents a differential architecture of CMOS transimpedance amplifier is offered to obtain the input capacitive load insensitive and the very minimum noise structure. The suggested TIA is dependent on the differential structure and composed of a regulated cascode block and a differential amplifier along with active feedback. To increase the bandwidth of the amplifier series inductive peaking and a capacitive degeneration step employed. Simulation results shows that the TIA achieves 100 GHz bandwidth, 80.4 dBΩ transimpedance gain, and 20 pA/
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**Index Terms**

Computer Science  
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**Keywords**

CMOS, Inductive series peaking, Transimpedance amplifier (TIA), Bandwidth enhancement, RGC, Capacitive degeneration, Active feedback.