Simulation of a Nanoscale SOI TG n-FinFET

International Journal of Computer Applications

Volume 138
Number 8

Year of Publication: 2016

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10.5120/ijca2016908981
{bibtex}2016908981.bib{/bibtex}

Abstract

The objective of this work is to study the electrical characteristics of a nanoscale SOI Tri-Gate n-channel fin field-effect transistor (FinFET) structure with 8 nm gate length using Semiconductor TCAD tools. ATLAS™ tools are computer programs which allow for the creation, fabrication, and simulation of semiconductor devices in three dimensions with different models under consideration. The drain current, transconductance, threshold voltage, subthreshold slope, leakage current, drain induced barrier lowering, and IOn/IOff current ratio are analyzed in the various biasing configuration. In addition, FinFET device with a high value of gate dielectric constant exhibits much better performance compared to the Si3N4 dielectric material, which is desirable for high performance low-power/low-voltage applications. It is found that increasing the high-k value was beneficial in reducing the subthreshold slope, DIBL, and leakage current.

References

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**Index Terms**

Computer Science | Circuits and Systems
Keywords

Device scaling, FinFET, SCEs, Leakage current, Silvaco Software.