Design and Simulation of OTA using DTMOS Technique in 180 nm CMOS Process

Volume 139

Number 7

Year of Publication: 2016

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Abstract

In this paper, a low voltage low power CMOS Operational transconductance amplifier using DTMOS technique is described. The OTA is designed and simulated with 0.18µm CMOS technology. Simulation results show that with DTMOS technique, the open loop gain is 23.05 dB, the unity gain bandwidth is 379.7 KHz, phase margin is 93.8 degree, power consumption is 1.397 µw and input noise is 25.71 nv2/Hz at 1 Hz frequency while operating at 0.6 v supply voltage and under 1 pF capacitor load. DTMOS technique provide low noise compared to conventional OTA. So DTMOS technique is suitable for low noise and low power applications such as biomedical applications.

References


Index Terms

Computer Science

Circuits and Systems

Keywords

DTMOS, OTA, open loop gain, unity gain bandwidth, phase margin.