Low Power and High Speed 13T SRAM Cell with Bit-Interleaving Capability

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Abstract

In this paper a low power single ended 13T SRAM cell has been proposed for bit inter-leaving application. A column aware scheme is used in the cell to achieve stable SRAM cell with better performance than the existing designs. The proposed SRAM cell exhibit robust read operation and better read performance with lower power consumption. This proposed 13T SRAM has been compared with standard 6T SRAM and existing 9T SRAM (with bit-interleaving capability) in term of Power consumption, Delay and Power Delay Product (PDP) at various supply voltages as 1.8V, 1.6V and 1.4V. The simulations are carried out on Cadence Virtuoso at 180nm CMOS technology and the simulation results are analyzed to verify the superiority of the proposed design over the existing designs. The proposed 13T SRAM proves to be better in terms of power and PDP at all the supply voltages. At 1.8V power saving by the proposed circuit is 72.46% compared to standard 6T SRAM cell and significant improvement is observed at other supply voltages also.

References

**Index Terms**

Computer Science  
Power Systems
Keywords

SRAM cell, Leakage Power, Low Power, Stability, Bit-interleaving, PDP.