Abstract

Embedded systems used in real-time applications require design tools that could be costly and may have long verification cycles. Many design tools use predefined libraries and costly IPs during these design and verification cycles, and most of these libraries and IPs are static and difficult to modify. Many design requirements are changed during or after design and verification cycle, and designers need to address these changes and modify the system. This could be more time consuming due to verification cycle and static libraries. It is important to have dynamic libraries that could be modified and reconfigured based on the applications. This work creates reconfigurable arithmetic design blocks that could be used for arithmetic and matrix operations. The reconfigured library development system modifies the required library elements using Perl scripting language and verifies them on-the-fly using MATLAB. The development tool improves design time and reduces the verification process, but the key point is to use a unified design that combines some of the basic operations with more complex operations to reduce area and power consumption. The results indicate that using the reconfigurable development tool reduces verification time and increases the productivity. These libraries include structural
Verilog HDL codes, testbench files, and MATLAB script files for local customization. Even though the reconfigurable HDL library is used for FPGA design flow, it could be easily modified for VLSI design flow.

References


Index Terms

Computer Science

Applied Mathematics

Keywords

Hardware optimized, HDL, High Level Synthesis, MATLAB, Optimized Hardware, Perl, Power Efficient, Reconfigurable, RTL, Verilog HDL.