Abstract

This paper presents low power full adder designed with pass transistor logic which reduces the area, power and delay. We compared conventional 28T CMOS full adder with 16T and 8T full adder in terms of area, power and delay using 45nm Technology.

The schematic of all three design has been developed and its layout has been created using micro-wind tool. The result show that 8T full adder consumes 98% less power as conventional 28T & 65% less power compared to 16T full adder.

References


Index Terms

Computer Science

Circuits and Systems

Keywords

Full adder, Pass Transistor logic (PTL), Transmission gate (TG), CMOS, Drive current, Channel Length.