In this paper a transposed FIR filter with 8, 16 and 32-tap with 16-bit inputs has been implemented with a new technique that is called differential input. This technique is beneficial in terms of the hardware cost and low power design. The common transposed FIR filter and its differential input one are simulated by Xilinx ISE tool and implemented on Spartan 6 FPGA. The achieved results show that the area and dynamic power of the proposed FIR filter with this technique are reduced. According to the results the dynamic power of the 16 and 32-tap FIR filter with this technique are reduced by 5.59% and 10.28% respectively.

References

Low Power FPGA Implementation of a Transposed Form FIR Filter with Differential Input Technique

Systems and Workshops (ICUMT), St. Petersburg, 2012, pp. 1002-1005.


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