Transistor Gating Technique: Designing of Full Subtractor Circuit Implementing Sleepy Transistors in 45 nm Technology

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Abstract

Full subtractor is a combinational circuit that performs subtraction between the three inputs and provides result in difference and borrow outputs. Implementing the MTCMOS technique on this circuit results in reduction of leakage current and power consumption. The proposed Full Subtractor has been designed and simulated using DSCH 3.1 and MICROWIND 3.1 software. The simulation technology used is 45 nm. The simulation level is BSIM advanced level. The proposed design power consumption calculated as 0.341 mW and maximum current Idd max equal to 2.420 mA at 0.7 Supply voltages.

References

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Index Terms

Computer Science  Circuits and Systems

Keywords

Full subtractor, MTCMOS, transistor gating, leakage current, power dissipation.