Design of Low Power Sense Amplifier based NAND Latch under 30nm Technology

Abstract

In electronics, a latch is a circuit that has two stable states and can be used to store information. Therefore latches can be memory devices and can store one bit of data as long as the device is powered. This paper mainly concentrated on the design of low power sense amplifier based NAND latch where sense amplifier is part of the read circuit that is used when data is read from the memory and amplify the voltage swing. An analytical model of different sense amplifier based NAND latch was designed and simulated using 30nm CMOS technology with various supply voltage. The NAND latch designed using low power Conventional Voltage Sense Amplifier is proposed in this paper. The simulation is carried out in SYNOPSYS EDA software under 30nm technology with different supply voltages.

References

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Index Terms

Computer Science
Circuits and Systems
Keywords

Memory, Sense Amplifier, NAND latch, Low Power.