In this paper a low power design for CMOS ring oscillator is proposed and analyzed for power consumption. The proposed design is compared with an existing design. The simulation is done on Cadence virtuoso tool at 180nm CMOS technology and the results are analyzed for power consumption. The proposed ring oscillator circuit uses positive feedback in its inverter based circuit and operate with nine cascading CMOS inverter. The power consumption of the proposed design is reduced by 28.40% at 0.9v and 54.64% at 1v as compared with a previous design.

References


Index Terms

Computer Science

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Keywords
CMOS inverter, ring oscillator, power consumption, leakage power.