Leakage Power Reduction by using Sleep Switches in Domino Logic Circuit Design in DSM Technology

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Abstract

Power consumption is hurdle problem face by nanometer CMOS circuit in deep submicron process (DSM) technology. As technology scales down, leakage power significantly increases very rapidly due to high transistor density, reduced voltage and oxide thickness. A new circuit technique based on: “Sleep Switch” is proposed in this paper for reducing the subthreshold and gate oxide leakage currents when circuit is operating in idle and non idle mode in domino circuit design. In this technique a p-type and an n-type leakage controlled sleep transistor are introduced between the pull-up and pull-down network and their gates are controlled by the source of the other. For any combination of input, one of the Sleep transistor will operate near cut off region which increase the resistance path between supply voltage and ground resulting in reduced leakage current. The proposed circuit technique reduces the active power consumption by 14.3% to 44.45% and by 12% to 33% at the low and high die temperature respectively compared to the standard footerless domino logic circuits. During idle mode, 11.64% to 78.39% and 21.2% to 36.19% reduction of leakage current is observed with low and high inputs at 250C and 1100C respectively. Similarly, during non-idle mode 0.94% to 99.3%
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and 1.57% to 98.58% is observed with low and high inputs at 25°C to 1100°C respectively when compared to standard footerless domino logic circuits.

References

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Index Terms

Computer Science  Power Electronics

Keywords

Domino logic; Evaluation Delay; Keeper transistor; Noise immunity; Robustness; Wide fan-in gate