Abstract

The multiplication operation is used in many parts of a digital system or digital computer, usually in signal processing, video/graphics and scientific computation. With advances in technology, various techniques have been developed to design multipliers, which offer high speed, low power consumption and lesser area. Thus making them suitable for various high speeds, low power compact VLSI implementations. These three parameters i.e. power, area and speed are always traded off. In this paper, different techniques used for efficient operations resulting in high speed and low power consumption are discussed. Such as parallelism, pipelining, modified booth algorithm (MBA), spurious power suppression technique (SPST), block enabling technique.

References

Techniques for the Design of High Speed and Low Power MAC Unit: A State-of-the-art Review


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Index Terms

Computer Science  Power Electronics

Keywords

Multiply and Accumulate (MAC), Modified Booth Algorithm (MBA), parallel modified booth multiplier, Spurious Power Suppression Technique (SPST), block enabling technique.