Performance Analysis of Different 8x8 Bit CMOS Multiplier using 65nm Technology

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ABSTRACT
In this paper different low power 8x8 bit multipliers which are implemented with Tanner Tool v13.0 at 250MHz and 500MHz frequency with 65nm technology which is having a supply voltage 1.0v. There are different CMOS multiplier circuits are analyzed which are Array multiplier, Wallace tree multiplier, Row bypass Braun multiplier, Column bypass Braun multiplier, Row and Column bypass Braun multiplier and these multiplier are realized using bridge style full adder. All these multipliers are compared in terms of delay, power dissipation and power delay product. Simulation results show that the Array multiplier and Wallace tree multiplier using bridge style adder has less power delay product and is faster as compared to other CMOS multipliers.

Keywords
CMOS, PDP, VLSI, Multiplier, Array multiplier, Wallace Tree, Braun bypass multiplier.

1. INTRODUCTION
Multiplication put up in a variety of applications in most of the Digital Signal Processing (DSP) applications. In high speed digital signal processing (DSP) and image processing multiplier play a vital role. With the rapid development of mobile computing and battery-powered system as well as the energy conservation consideration, low power VLSI design has become a very important issue in the VLSI industry. Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, increase cost, and decrease system reliability.

[1] The multiplier is the arithmetic operation unit for microprocessors and many DSP applications, such as filtering, convolution, Fast Fourier Transform (FFT), etc [2].

Hence, it is very important to develop low-power multipliers to enhance the performance of overall system. Therefore low-power multiplier design has been an important part in low-power VLSI system design. Also these low power design systems reduce cooling cost and increase the reliability of high density designs. With the recent advances in technology, many researchers have tried to implement increasingly efficient multiplier. They aim at offering low power consumption, high speed and reduced delay. [3]. This paper proposes and evaluates the technique to reduce the power dissipation of multipliers. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level.

A number of approaches have been adopted to implement a multiplier circuit with low transistor count, low power consumption, high speed etc. The basic and typical array multiplier performs multiplication by arranging the full-adders to add the partial products for each output bit [4].

Power dissipation is the most important parameter for CMOS circuits and it is classified into dynamic and static power dissipation. Dynamic dissipation is due to charging and discharging load capacitances as gates switch and “short-circuit” current while both pMOS and nMOS stacks are partially ON [5]. Static dissipation is due to sub threshold leakage through OFF transistors, gate leakage through gate dielectric, and junction leakage from source/drain diffusions.

Putting this together gives the total power of a circuit

\[ P_{tot} = P_{dynamic} + P_{leakage} = V^2 \cdot f_{clk} \cdot C_L \cdot \alpha + \alpha/12 \cdot (V_{dd} - 2V_{th})^3 \cdot t_r/t_f + I_{leakage} \cdot V_{dd} \]

Where \( f_{clk} \) is the system clock frequency, \( C_L \) is the load capacitance, \( \alpha \) is the switching activity factor, \( t_r \), \( t_f \) is the rise and fall time of input signal. \( I_{leakage} \) is the total leakage current flowing through the device. The dynamic power of CMOS circuits is becoming a major concern in the design of devices [6]. In this paper we optimize the dynamic power of multiplier circuits.

In this paper low power Array multiplier, Wallace tree multiplier and Braun multiplier with bypassing techniques are presented and modified adder module is implemented for a low power high speed multipliers. The full adder circuit is basic block of multiplier circuit. In these multiplier bridge style full adder cell [13] is used which has less power dissipation as compare to static adder.

2. MULTIPLIER ARCHITECTURE
The multipliers have a predominant effect on the system performance, many high performance algorithms and architectures have been proposed [7]. Some of architecture of multipliers are explained below:

2.1 Array multiplier
Braun multiplier is a simple parallel multiplier and it is generally known as carry save array multiplier and in a \( n \times n \) bit Braun multiplier, the multiplier array consists of (n-1) rows of carry-save adders (CSAs) and a (n-1) bit ripple-carry adder in the last row, in which each row contains (n-1) full adder (FAs). Array multiplier has a regular structure. It is easy
to layout and also it has small size. The design time of an array multiplier is much less than other multipliers [8].

Fig.1: 4×4 bit Braun multiplier

2.2 Wallace tree multiplier
In Wallace tree multiplier architecture, all the bits of all of the partial products in each column are added together by a set of adders in parallel without propagating any carries. The entire procedure is carried out into three steps: partial product (PP) generation, partial product grouping & reduction, and final addition. [9].

Fig.2: Dot diagram of 4-bit Wallace tree multiplier

In a Wallace multiplier, the number of partial products generated is the same as in the Array Multiplier. Thus there are still N^2 AND gates required for an N-bit by N-bit multiplication. The main disadvantage of Wallace multiplier is its irregular layout. Due to used carry-save operations, it reduced the delay time.

2.3 Braun Multiplier with Row Bypassing
The particular rows of adders is bypassed when the multiplier bit is zero in the basic multiplier array in Row bypassing technique to save the switching power. The Braun multiplier with row bypassing uses additional three tri-state buffers and two 2-to-1 multiplexers and these are attached to FA cell [10]. The extra correcting circuits must be added in this multiplier to correct the multiplication result.

Fig.3: 4-bit Braun Multiplier with Row Bypassing

2.4 Braun Multiplier with Column Bypassing
In column bypassing technique an addition operation of column can be disabled if the corresponding bit in the multiplicand is 0. In this multiplier FA is only attached by two tri-state buffers and one 2-to-1 multiplexer [11], so the modified FA is simpler than that of used in the row bypassing multiplier.

Fig.4: 4-bit Braun Multiplier with Column Bypassing
It also eliminates the extra correcting circuit. So it uses less hardware as compare to row bypass multiplier.

2.5 Braun Multiplier with Row and Column Bypassing
In Row and Column Bypassing technique the addition operation in the (i+1)-th column or the j-th row can be bypassed if the bit, ai in the multiplicand is 0 or the bit, bj in the multiplier is 0. In this the (i+1, j) FA can be bypassed if the product, ai bj, is 0 and the carry bit, ci,j-1, is 0, that is, as the product, ai bj, is 1 or the bit, ci,j-1, is 1, the addition operation in the (i+1, j) FA can be executed [12]. Simplification of full adders is done for the addition operation. The simplified adder, A+1, in the CSA array is attached by one tri-state buffer and two 2-to-1 multiplexers and simplified adder, A+B+1, in the CSA array is attached by two tri-state buffers and two 2-to-1 multiplexers.
3. PROPOSED MULTIPLIER DESIGN

In this paper, we design and analyze different multiplier with bridge style full adder cell [13]. It has the less PDP as compared with conventional static adder. Due to the minimum time delay of sum and carry out, the adder enhance the overall performance of multipliers. Circuit diagram of full adder, sub circuits and different multiplier design are shown in Fig. 7 to Fig. 17.
Fig. 13: Circuit Diagram of 8-bit Array multiplier

Fig. 14: Circuit Diagram of 8-bit Wallace tree multiplier

Fig. 15: Circuit Diagram of 8-bit Row Bypass Braun Multiplier

Fig. 16: Circuit Diagram of 8-bit Column Bypass Braun multiplier
4. SIMULATION RESULTS

Simulations are performed using 65nm CMOS technology. Spice simulation are carried out with supply voltage 1V and at different frequency 250MHz and 500MHz. For all possible input combination sets applicable to the multiplier, I have calculated the average power consumption, delay, and power delay product. All result of different multipliers are summerised in the form of table which are described below:

Table 1: Average Power Dissipation, Delay and PDP comparison of 8-bit multiplier at 250MHz

<table>
<thead>
<tr>
<th>Type of Multiplier</th>
<th>Power (mw)</th>
<th>Delay (ns)</th>
<th>Power Delay Product (pJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td></td>
<td></td>
<td>250Mhz</td>
</tr>
<tr>
<td>Array Multiplier</td>
<td>5.435</td>
<td>9.761</td>
<td>53.051</td>
</tr>
<tr>
<td>Wallace Tree Multiplier</td>
<td>5.403</td>
<td>9.792</td>
<td>52.906</td>
</tr>
<tr>
<td>Row Bypassing Braun Multiplier</td>
<td>24.121</td>
<td>7.647</td>
<td>184.453</td>
</tr>
<tr>
<td>Column Bypassing Braun Multiplier</td>
<td>11.496</td>
<td>9.625</td>
<td>110.649</td>
</tr>
<tr>
<td>Row and Column Bypassing Braun Multiplier</td>
<td>25.735</td>
<td>9.751</td>
<td>250.942</td>
</tr>
</tbody>
</table>

Table 2: Average Power dissipation, Delay and Power Delay Product comparison of 8-bit multiplier at 500MHz.

<table>
<thead>
<tr>
<th>Type of Multiplier</th>
<th>Power (mw)</th>
<th>Delay (ns)</th>
<th>Power Delay Product (pJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td></td>
<td></td>
<td>500Mhz</td>
</tr>
<tr>
<td>Array Multiplier</td>
<td>10.076</td>
<td>4.766</td>
<td>48.022</td>
</tr>
<tr>
<td>Wallace Tree Multiplier</td>
<td>10.029</td>
<td>4.798</td>
<td>48.119</td>
</tr>
<tr>
<td>Row Bypassing Braun Multiplier</td>
<td>31.757</td>
<td>3.657</td>
<td>116.135</td>
</tr>
<tr>
<td>Column Bypassing Braun Multiplier</td>
<td>20.313</td>
<td>4.635</td>
<td>94.151</td>
</tr>
<tr>
<td>Row and Column Bypassing Braun Multiplier</td>
<td>33.206</td>
<td>4.749</td>
<td>157.695</td>
</tr>
</tbody>
</table>

Table 3: Transistors Count of different 8-bit multipliers

<table>
<thead>
<tr>
<th>Type of Multiplier</th>
<th>Transistor Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array Multiplier</td>
<td>1952</td>
</tr>
<tr>
<td>Braun (Array) Multiplier</td>
<td>1648</td>
</tr>
<tr>
<td>Wallace Tree Multiplier</td>
<td>1648</td>
</tr>
<tr>
<td>Row Bypassing Braun Multiplier</td>
<td>5046</td>
</tr>
<tr>
<td>Column Bypassing Braun Multiplier</td>
<td>3622</td>
</tr>
<tr>
<td>Row and Column Bypassing Braun Multiplier</td>
<td>4196</td>
</tr>
</tbody>
</table>

Fig. 17: Circuit Diagram of 8-bit Row and Column Bypass Braun multiplier

5. CONCLUSION

This paper analysis comparative study of some of the well known existing multiplier named as Braun multiplier, Wallace tree multiplier, Row bypass Braun multiplier, Column bypass...
Braun multiplier and Row and Column bypass Braun multiplier using bridge style one bit adder. All circuit logic style is designed using different gate width of NMOS and PMOS and with a minimum length of 65nm for NMOS and PMOS by using Tanner V13 Tool. The multipliers using bypassing technique have much higher transistor count as compared to Array and Wallace tree multiplier but have less delay. So these different multipliers still perform worse in terms of power and power-delay product compared to the basic array multiplier.

6. REFERENCES


