A Study on Applying Parallelism for Construction of Steiner Tree Algorithms in VLSI Design

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Abstract

We present a survey of the different approaches that can be parallelized and also the parallel algorithms available today with special concern to Rectilinear steiner tree for VLSI Design and their appropriateness for high-performance computing. Thus, we review the parallel algorithms for solving the Steiner tree problem as it is of great importance for very large scale integration routing and wire length estimation. As the steiner problem in general is NP-hard, it is difficult to develop a polynomial-time algorithm to solve the problem exactly. This is why the most of research has looked at finding efficient heuristic algorithms. Additionally, many authors focused their work on utilizing the ever-increasing computational power and developed many parallel methods for solving the problem. Hence we are able to obtain better results in less time than ever before. The study shows that the accessibility of multi-core CPUs has given new impulse to the shared memory parallel programming approach. Hybrid parallel programming is the current way of harnessing the capabilities of computer clusters with multi-core nodes. On the other hand, high performance heterogeneous programming is found to be an increasingly well accepted paradigm, as a result of the availability of multi-core CPUs and GPUs systems. The
use of open industry standards like OpenMP, MPI, or OpenCL, as opposed to proprietary solutions, seems to be the way to categorize and extend the use of parallel programming models. Here, we present a survey of the parallel methods for solving the Steiner tree problem specifically for VLSI design.

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**Index Terms**

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**Keywords**

RSMT, OARSMT, Multicore Architecture