Abstract

The architectural advancements in desktop computing have made embedded devices in real time applications to adopt multi core architectures. The main challenge in multi core programming is the process of communication between the different executing cores. Effectiveness of parallel programming in multi core architectures lies in method used for communication. Communication using shared cache is one of the popular approaches. This paper discusses in detail one of the novel methods of inter core communication. Correctness of the algorithm has been based on results obtained on a hard real time system.

References

2. Shin’ichi Miura, Toshihiro Hanawa, TaisukeBoku, Mitsuhisa Sato: XMCAPi: Inter-Core

3. HengQuan, Ruijing Xiao, Kaidi You, Bei Huang, Xiaoyang Zeng, Zhiyi Yu.: A Simple High-Efficient Inter-Core Communication Mechanism for Multi-Core Systems, State Key Laboratory of ASIC and System, Fudan University, Shanghai.


8. Longfei Tan , Zhao Han,Chunguang Chen,Yinghua He ; Kunlong Zhang : A Non-blocking Self-Organizing Linked List Algorithm, Parallel and Distributed Computing, Applications and Technologies (PDCAT), 2012 13th International Conference, pp. 71-76, 2012


Index Terms

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Keywords

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