Abstract

Many of the today’s real time signal processing algorithm included multiplication as its processing heart. In case of signal and image processing, it mostly used functional unit. In this paper we are simulating different multiplication algorithm with their effective architecture. Also paper introducing new multiplication technique using barrel shifter which gives some sort of modification in previously described shift and add multiplication algorithm. Research targeting mainly four algorithms as Vedic vertical crosswise multiplication algorithm, Array multiplier, Shift and add multiplier, Wallace tree multiplier. Further work will carried comparative study of different multiplier with respect to some parameters like logical resources used, delay, power consumption and area. For implementation and parametric analysis, experimental setup uses sparten-3 XC3S400 FPGA as a hardware platform, VHDL coding language for hardware description. Xilinx ISE-simulation tool has many inbuilt compatible facility for parameter analysis like XPE for power analysis. Finally Paper comprises simulation results for 8-bit, 16-bits and 32-bits each of above mentioned multiplier.
FPGA Implementation and Analysis of Different Multiplication Algorithm

References

2. Cem Ergun, seminar at Eastern Mediterranean University on “Multiplication & Division Algorithms”.

Index Terms

Computer Science

Algorithms
Keywords

Array multiplier, Vedic, Wallace tree, shift and add, Barrel shifter.