As CMOS technology downsized into double digit nanometer ranges, variations are a serious concern due to uncertainty in devices and interconnect characteristics. The single event upset (SEU) is changing the state of a memory cell due to the strike of an energetic particle. The single event multiple effects are likely to increase in nanometer CMOS technology due to reduced device size and scaling of power supply voltage. SRAM cells are sensitive to radiation induced hazards. Therefore, designing a reliable novel SRAM cell is an important challenge against SEU. In this paper, the proposed SRAM cell that provides a better features than their recent proposed SRAM cells. The simulation results and analysis represent that the proposed SRAM cell exhibits the high robustness against single event multiple effects (SEMEs). Moreover, the proposed SRAM cell successfully reduced the power consumption by 41% and write delay by 2% in comparison with the existing radiation-hardened SRAM cells at the cost of circuit complexity. The process corner analysis displays the comparison of power and delay of the proposed and existing SRAM cells. It shows that the proposed memory cell consumes less power than previous memory cells.
References


**Index Terms**

Computer Science                Circuits and Systems

**Keywords**

Single event upset (SEU), Single event multiple effects (SEMEs), Single event multiple upset (SEMU), Radiation hardened dynamic (RHD) SRAM cell