A Novel circuit of SRAM Cell Against Single-Event Multiple Effects for 45nm Technology

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ABSTRACT

As CMOS technology down sized into double digit nanometer ranges, variations are a serious concern due to uncertainty in devices and interconnect characteristics. The single event upset (SEU) is changing the state of a memory cell due to the strike of an energetic particle. The single event multiple effects are likely to increase in nanometer CMOS technology due to reduced device size and scaling of power supply voltage.SRAM cells are sensitive to radiation induced hazards. Therefore, designing a reliable novel SRAM cell is an important challenge against SEU. In this paper, the proposed SRAM cell that provides a better features than their recent proposed SRAM cells. The simulation results and analysis represent that the proposed SRAM cell exhibits the high robustness against single event multiple effects (SEMEs). Moreover, the proposed SRAM cell successfully reduced the power consumption by 41% and write delay by 2% in comparison with the existing radiation-hardened SRAM cells at the cost of circuit complexity. The process corner analysis displays the comparison of power and delay of the proposed and existing SRAM cells. It shows that the proposed memory cell consumes less power than previous memory cells.

Keywords

Single event upset (SEU), Single event multiple effects (SEMEs), Single event multiple upset (SEMU), Radiation hardened dynamic (RHD) SRAM cell

1. INTRODUCTION

As technology size moving toward nanometer size, new circuits have been proposed. The normal operation of logic cells changed due to soft errors caused by the radiation effects. As technology scales, memory elements used with in the logic blocks become vulnerable to soft errors. Storage elements like conventional SRAM, flip flop (FF), latch circuits become more sensitive to SEU induced by effect of radiation [1]-[4]. An ionizing particle striking a cell of memory, due to this the value stored in the memory cell gets altered and results in failure of logic cell operation. This state change of a memory cell due to the strike of an energetic particle is called SEU [5]-[7]. When an energetic particle striking a gate or a chip may affect multiple sensitive nodes in a circuit through charge sharing and produces bit flip at each node. Therefore single event produces multiple effects this phenomenon is called SEME and it causes a multiple bit flips in the memory cell is called single event multiple upset (SEMU) [8]-[10].
As CMOS emerges into nanoscale technology SEMEs and SEMU are the main effects of energetic particle strikes due to radiation issues [11]. In this technology, mainly focused on circuit level techniques to point out the SEMEs concern. In circuit level techniques, designer concentrated on robust SRAM cell. Even though an energetic particle striking multiple nodes of a cell, the resultant logic operation of the cell would not change and hence there is no value is altered inside the memory cell [12]-[16]. In this paper, the proposed SRAM cell that can be used in different design techniques. The proposed SRAM cell provides low average power and delay and it has a much more critical charge than their previous radiation-hardened SRAM cells. It offers a high robustness against the single event multiple effects at the expensive of four more transistors. Power and delay analysis shown in section 5.
The remainder of the paper is structured as follows. Section 2 presents the particle strike injection. Section 3 describes the existing RHD SRAM cells. Section 4 depicts the proposed novel SRAM cell. Section 5 examines the proposed SRAM cell circuit design and differentiates it with the existing RHD SRAM cells. Finally, conclusions are shown in section 6.

2. PARTICLE STRIKE INJECTION MODELING

In a SRAM cell, the single event upset (SEU) will occur, when the charge deposited at the struck node by the energetic particle strike is greater than the critical charge stored in that node. The critical charge for a logic circuit can be defined as the minimum amount of charge required at a node in the circuit to alter the stored value in the memory cell, when the charge deposited in that node. Critical charge is typically characterized on a node basis only. The phenomenon of energy particle striking the CMOS devices has been studied by the researchers [17]. This may be modeled as a time varying double exponential current pulse.

$$I_{inject}(t) = \frac{Q_{inject}}{\tau_\alpha - \tau_\beta}(e^{\frac{-t}{\tau_\alpha}} - e^{\frac{-t}{\tau_\beta}})$$

Where Q_{inject} is the amount of injected charge in the struck region,and τ_α and τ_β are material dependent time constants. The time constants for the exponentials depend on several factors, the time constants given in [18] as τ_α=$1.64 * 10^{-10}$sec and τ_β =$5.0 * 10^{-11}$

sec. To simulate the energetic particle strike at a node, a current source $I_{inject}(t)$ is applied to that node. Where $I_{inject}(t)$ is considered as a charge applied on the struck node region as a SEU.

3. EXISTING RHD SRAM CELLS

The existing radiation hardened dynamic (RHD SRAM cells displayed in the Fig. 1 and 2. The circuits named as RHD11 (Fig. 1) and RHD13 (Fig. 2). In RHD11 circuit, when refresh line (RL) =0, the circuit offers full immunity to SEU. Otherwise, it shows an effect on adjacent nodes, due to that effect stored value altered in the memory cell. It can tolerate any particle strike at any node in the circuit in presence of RL=0 and the result would not change. If an energetic particle strike at the double node pair, the value stored in the memory cell is altered. The RHD11 circuit is quite robust against SEMEs. The RHD11 and RHD13 circuit proposed by the authors of [19], the RHD13 gives better robustness against SEMEs as compared with RHD11. RHD13 get the higher critical charge at node X1 than RHD11 with the help of addition of two more transistors N7 and P5. The switching threshold voltage of N3 and P4 is more as compared with the N4 and P3. If the particle strikes at the double node pair that noise voltage is filtered by the latch element (P3, P4, N3, and N4). Therefore RHD13 can tolerate even if an energetic particle strikes affecting double nodes, and it gives high robustness against SEMEs as compared with RHD11 [19].

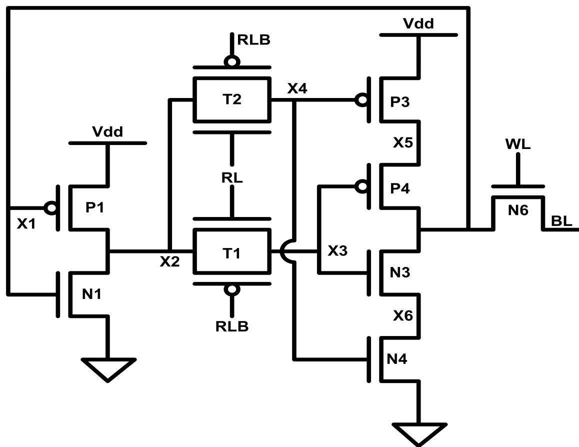

Fig. 1. Schematic of RHD11 memory cell.

4. PROPOSED ROBUST SRAM CELL

As MOS devices, scaling towards nanometer ranges SEMEs are big problems in circuit design techniques. Therefore, robust SRAM cells have to be designed against SEMEs induced by radiation effects. The succeeding section propose a novel SRAM cell which provides a better robustness against SEMEs and that require low power and delay as compared with the previous RHD SRAM cells.

4.1 Proposed Radiation Hardened SRAM Cell

The proposed SRAM cell consists of 17 transistors is present in the Fig. 3. The operation of the proposed SRAM cell is similar to existing SRAM cells is shown in figure [Fig. 6], the N6 transistor is acting like access transistor is controlled by word line (WL), when RL =1 transmission gates T1 and T2 are providing the feedback loop from the inverter (P1, N1) to latch element (P3, P4, P5, N3,

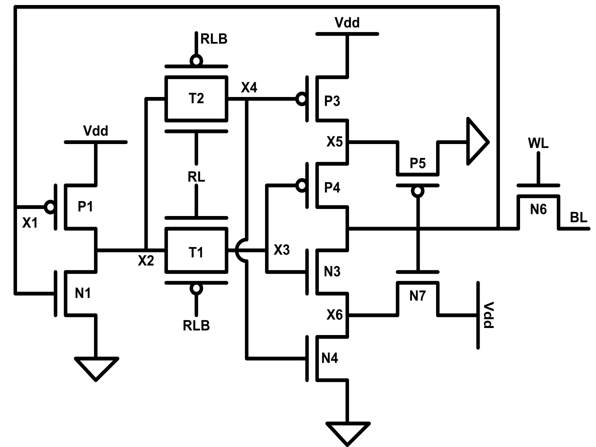

Fig. 2. Schematic of RHD13 memory cell.

N4, and N5) and it also disconnects the feedback loop between inverter and latch element in case of RL =0. Suppose consider a case if bit line (BL) is 1 and word line (WL) is assumed to be high then X1 node has a value 1 and its causes N1 transistor to turn ON. So X2 node gets a value to be 0 from the ground. As RL =1 both T1 and T2 becomes ON, X3 and X4 nodes get 0 value. Therefore P3 and P4 gets turned ON and X7 node gets approximately the V_{dd} voltage.

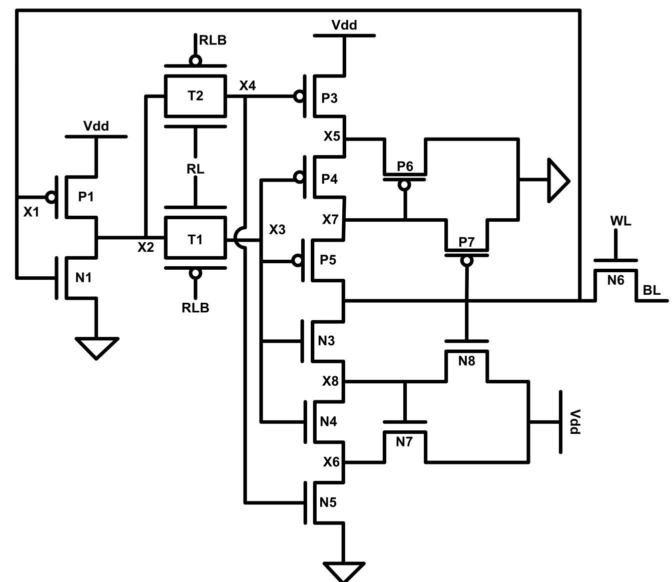

Fig. 3. Schematic of proposed memory cell.

When both WL and RL are low, then SRAM retains its data until the read operation. The stored value may be lost, if the feedback loop is left open. To rectify this problem, the control signal 'RL' of the transmission gates should go to 1 whenever the feedback loop is open. In this case any particle striking at the node X1 or X2, results will not show any effect on nodes X3 and X4. Let us consider a case BL =1, WL and RL are high, then X2 node at 0 value, T1 and T2 are ON then X3 and X4 nodes at 0. PMOS devices in latch elements are ON and X1 node charges to V_{dd} voltage (logic high) at that time

transistor N8 and N7 are going to turn ON, with the help of N8 and N7 biasing is provided at the nodes X8 and X6. The voltage values

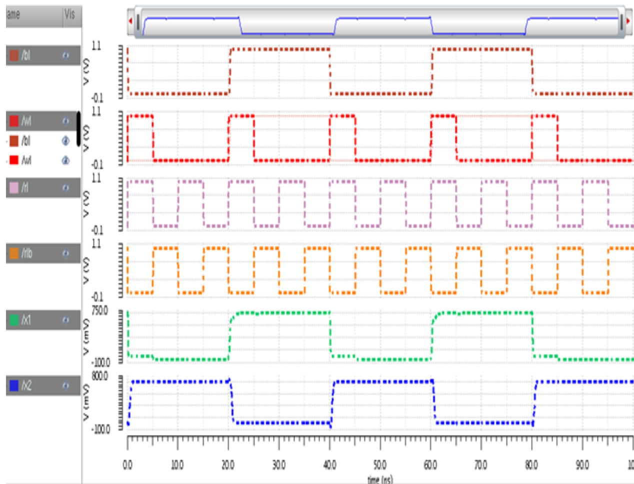

Fig. 6. The simulation results of the proposed SRAM cell.

at nodes X8 and X6 is assumed to be (V_{dd}-V_{th}) and (V_{dd}-2V_{th}). If an energetic particle strikes at node X2, the results will transmit through the transmission gates. The voltage at X3 node is V_n then N5 transistor is turned ON, when the voltage (V_{dd}-2V_{th}) at node X6 is dropping to a value of V_n through N5 then N4 is turned ON. Therefore the switching threshold voltages require for N3 and N4 is higher than N5. Therefore, in this latch element noise voltages are filtered. In this case the critical charge at the node X1 is increasing with adding of four transistors (N7, N8, P6, and P7). In case of BL =0, the reverse operation is performed, the critical charge obtained at the nodes in the proposed circuit is higher than the critical charge obtained in the existing RHD SRAM cells. Therefore, the proposed SRAM cell shows the high robustness against single event multiple effects in the presence of radiation effect.

5. COMPARISON OF RHD SRAM CELLS

In memory cell design, designers mainly concentrates on low cost, area, power consumption and better performance. To achieve high robustness and reliability there may be a chance of increase in the circuit complexity. The comparison between the proposed and existing SRAM cells performed and simulated by CADENCE Virtuoso tool using 45nm technology, supply voltage set to 0.7V and temperature set to 25^0C, at process corner analysis temperature set to 80^0C and -40^0C.

Table 1. Comparison of 45nm SRAM cell parameters

Parameters	RHD11	RHD13	Proposed
Power(nW)	139.4	149.7	87.82
Write delay(ns)	20.7	20.72	20.22
read delay(ns)	20.19	20.18	20.19

Table I and Table II represent the average power consumption, performance and critical charge at the circuit nodes of the proposed SRAM cell together with the noticed values of existing memory cells. Table I depicts that the proposed SRAM cell has low power and delay and it requires more area as compared with previous

Table 2. Critical charge for various nodes in the SRAM cells when RL =1

SRAM Type	Node	Critical Charge(Q_c)($10^{-22}C$)
RHD11	X1	4.71
	X2	14.51
	X5	10.50
	X6	3.26
RHD13	X1	7.01
	X2	16.26
	X5	14.09
	X6	4.37
Proposed	X1	11.65
	X2	18.91
	X5	22.37
	X6	7.91
	X7	41.66
	X8	10.22

memory cells. Table II represents that the proposed SRAM cell has a high critical charge in its circuit nodes, high robustness than the previous memory cells.

The simulation results obtained from the process corner analysis are shown in Fig. 4 and Fig. 5. At different temperatures, the proposed and existing SRAM cells exhibit different power and delay at different corners [20]. Comparison of power and delay for SRAM cells at temperatures 80^0C and -40^0C are displayed in Fig. 7 and Fig. 8. In process corner analysis, the proposed design has compa-

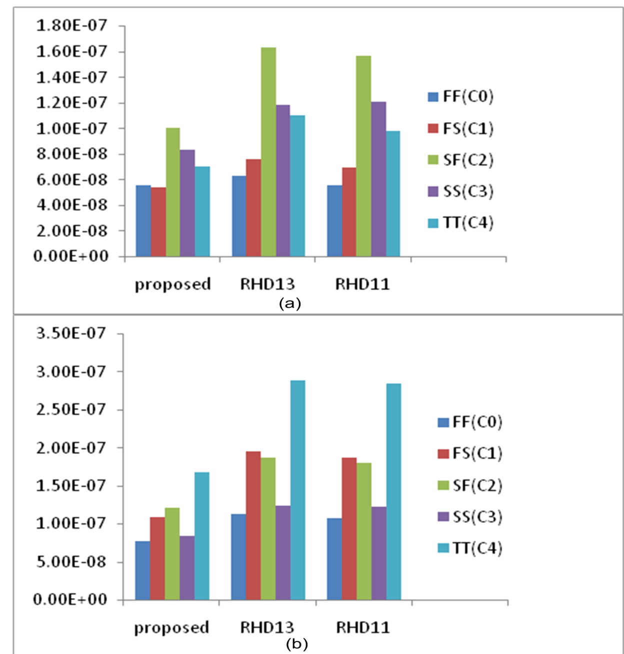

Fig. 7. Comparison of power for SRAM cells at temperatures (a) 80^0C and (b) -40^0C.

rable delay and consumes less power than previous designs.

6. CONCLUSION

Previous radiation hardened SRAM cells requires an increase of power consumption and write delay. This paper has given a novel

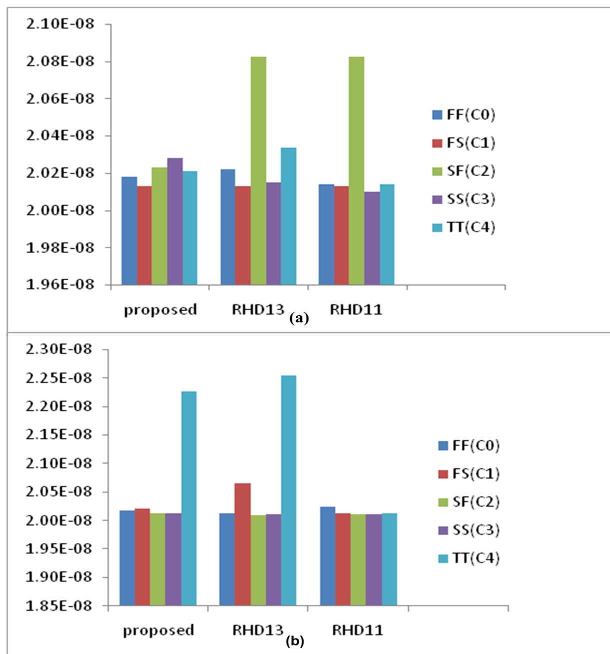

Fig. 8. Comparison of delay for SRAM cells at temperatures (a) 80^0C and (b) -40^0C.

immune SRAM cell. Using CADENCE Virtuoso tool, simulation analysis and results exhibited that, proposed SRAM cell presents better robustness against SEMEs and SEMU than their latest proposed designs (RHD11 and RHD13). It exhibits best dual node upset tolerance and it provides extraordinary performance (low power consumption and write delay) in comparison with the existing designs. Process corner analysis proved that at different temperature the power consumed at different corners in proposed memory cell is lower than the existing RHD SRAM cells. This paper has additionally displayed that the critical charge obtained in the proposed circuit nodes is higher than the existing memory cells. Therefore, the proposed SRAM cell provides a high robustness.

7. REFERENCES

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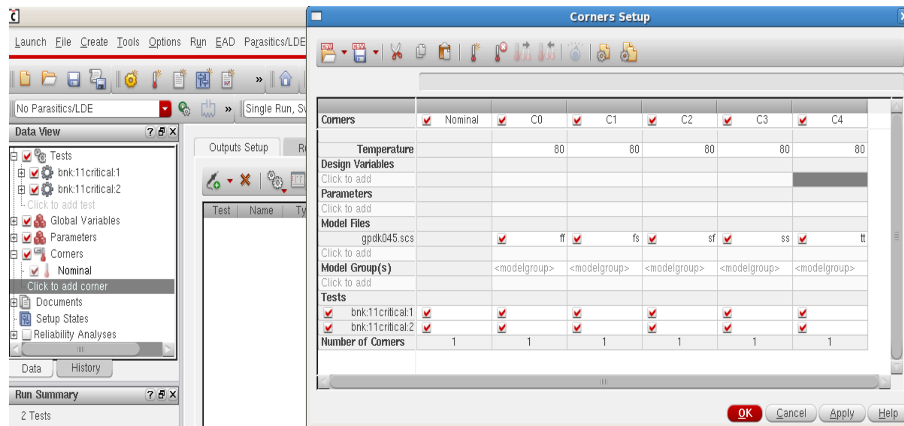

Fig. 4. Corners setup in process corner analysis at temperatures 80^0C.

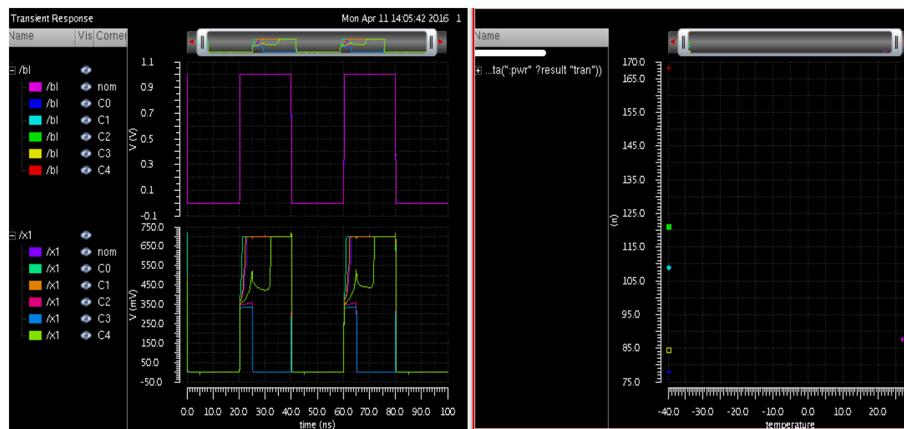

Fig. 5. Power measurement at different corners for SRAM cell.