Enhancement of the Performance of TFET using Asymmetrical Oxide Spacers and Source Engineering

Gihan T. Sayah
Assistant Professor of
Electronic Engineering
Nuclear Material Authority
Cairo, Egypt

ABSTRACT
In this paper, some techniques to enhance the performance of the tunneling field effect transistor (TFET) devices are studied. Two proposed techniques, which could be used simultaneously to improve the performance of TFET, are presented. The first technique is using different oxide materials for the spacers over the drain and source. The second technique is to select a different material of the source other than Si. The study is based on the DC I_D-V_{GS} characteristics as well as the high frequency characteristics regarding the capacitance and cut-off frequency. It was found from this study, that it is advantageous to use different materials for the spacers. The materials chosen for this work are HfO_2 as the spacer over the source and SiO_2 over the drain. It is also shown that using Ge as a source material provides the best performance. The criterion of the choices presented in this paper is based on providing higher ON current and lower ambipolar current and higher cut-off frequency.

General Terms
TFET, Simulation, Silvaco

Keywords
TFET, Ambipolar current, Spacers, Cut-off frequency.

1. INTRODUCTION
Advanced complementary metal–oxide–semiconductor CMOS technology now faces two problems [1] that together lead to high power consumption. The first issue is the increasing difficulty in further reducing the supply voltage. The other one is stopping the rising leakage currents that degrade the switching ratio of 'ON' and 'OFF' currents [2]. In a MOSFET, the current-switching process includes the thermionic injection of electrons [3, 4] over an energy barrier. This sets a fundamental limit to the abruptness of the transition slope from the OFF to the ON state. The charge carriers are thermally injected over a barrier in MOSFETs. Meanwhile, the interband tunneling is the main injection mechanism in a TFET. In this interband tunneling, charge carriers transfer from one energy band into another at a heavily doped p+n+ junction [5]. TFET is a new type of transistor whose fundamental switching mechanism differs from the conventional MOSFET. Its pronounced features make it a promising candidate for low-energy electronics.

The switching of TFETs is performed by modulating quantum tunneling through a barrier. This technique is different from that of conventional MOSFETs which is based on modulating thermionic emission over a barrier. Accordingly, TFETs are not limited by the thermal tail of carriers, which limits the subthreshold swing of MOSFETs to 60 mV/dec at room temperature [6]. TFETs have been proposed as a replacement of the conventional MOSFETs for low power applications as they are characterized by low leakage currents, better immunity to short channel effects (SCE) and compatibility with the CMOS process [7-9]. Meanwhile, TFET suffers from two fundamental problems: a low ON state current and ambipolar conduction. Some,.improvements have been proposed to overcome these challenges. Using a PNPN TFET with a source pocket, instead of the conventional p-i-n structure, can solve the problem of low ON current [10]. However, the problem of ambipolar conduction in TFETs limits their applications especially for digital circuit applications [11].

To overcome the ambipolar conduction, several device structures including gate-drain underlap, low drain doping have been proposed [11-13]. Although these methods decrease ambipolar current, they can only be grasped at the cost of increased fabrication complexity and reduced ON current. Recently, a gate-on-drain overlap method was proposed to control ambipolar conduction of TFETs [14]. However, increasing the overlap length results in higher capacitance effects which, in turn, leads to poor high-frequency characteristics [15].

In this work, two techniques are provided to reduce the ambipolar current without deteriorating the performance of the high-frequency switching characteristics. The first technique is based on choosing different materials for the source instead of Si. Two choices are provided; Ge and InAs. The second technique relies on choosing different oxide materials over the source and drain. Two different oxide materials are chosen: HfO_2, Sio_2.

The rest of the paper is organized as follows. In Section 2, the device structure and its parameters are introduced. Then, in Section 3, the simulation tool is reviewed along with its simulation parameters. Furthermore, the results are presented in Section 4. Finally, the conclusions are highlighted in the last section.

2. DEVICE STRUCTURE AND SIMULATION PARAMETERS
Fig. 1 shows a schematic of the TFET structure. The source and spacers materials will be changeable to study the effect of different source and spacers materials on the TFET characteristics. Ge, InAs and Si are used as source materials while SiO_2 and HfO_2 are used as spacers' materials. The parameters used for the device simulations are listed in Table 1. The channel, source and drain lengths are taken to be 50 nm, while the spacers' lengths are taken to be 10 nm. The BOX thickness is chosen to be 50 nm and the oxide thickness is 2 nm. The oxide thickness is equivalent to an effective oxide thickness EOT = 2 nm for SiO_2 whereas EOT = 0.4 nm for HfO_2. The silicon SOI thickness is t_{si} = 10 nm.

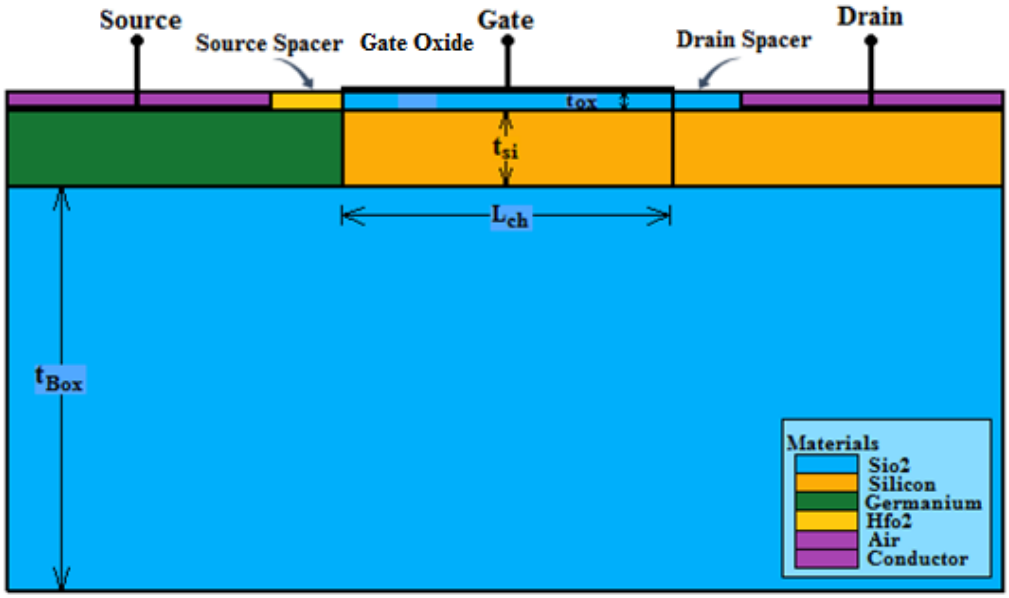


Fig. 1 Schematic of TFET structure

Table 1. Parameters used for the device simulations

Parameter	Value
Source Length	50 nm
Channel Length	50 nm
Drain Length	50 nm
Spacers Length	10 nm
Box thickness (t_{Box})	50 nm
Oxide thickness (t_{ox})	2 nm
t_{Si}	10 nm
Source doping	10^{20}
Drain doping	10^{19}
Channel doping	10^{17}

Fig. 2 shows the doping profile of the structure where the doping of the channel is taken to be 10^{17} cm^{-3}, the drain doping is 10^{19} cm^{-3} while the source doping is 10^{20} cm^{-3}.

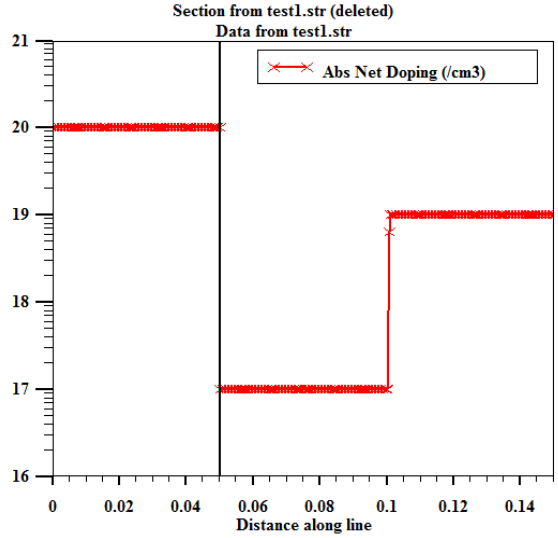


Fig. 2 Doping profile of the TFET (on a semilog scale)

3. SIMULATION AND DISCUSSION

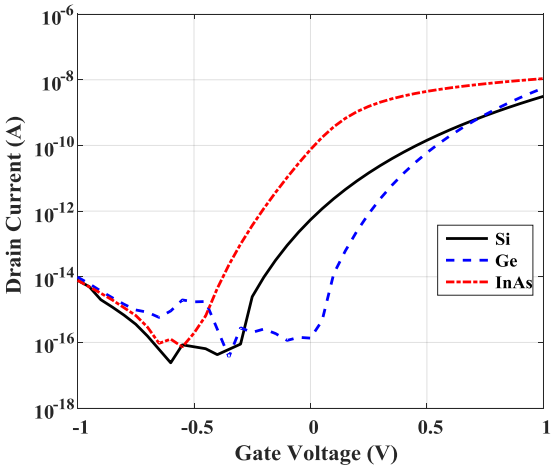
All the simulations were carried out using Silvaco Atlas [16]. Atlas is a physically-based two and three-dimensional device simulator that predicts the electrical behavior of semiconductor devices at specified bias conditions. Kane band-to-band tunneling (BTBT) model [17] was used to account for the tunneling in the lateral direction. Kane model is used to evaluate the band-to-band generation rate according to the following [18]

$$G_{btb} = \frac{|E|^2}{\sqrt{E_g}} \exp\left[-B\frac{E_g^{3/2}}{|E|}\right] \quad (1)$$

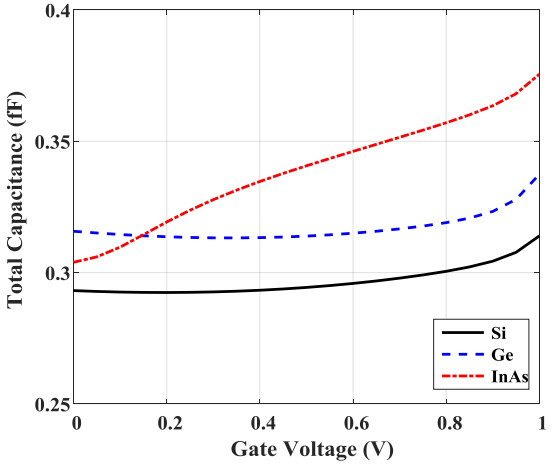
In this expression, $|E|$ is the magnitude of the electric field, and E_g is the energy band gap. The parameters A and B are constant parameters. G_{btb} is obtained from the magnitude of the electric field at each node considering local band-to-band tunneling model. The parameters for Kane's band-to-band tunneling in Silvaco Atlas, (A= 4×10^{19} $eV^{1/2}$/cm-s-V^2 and B = 41 MV/cm-$eV^{3/2}$). These parameters were chosen according to the calibration performed in [18] and calibrated with the

experimental results in [19]. Lombardi mobility model was enabled to account for high field mobility effects. Fermi-Dirac statistics and the Shockley-Read-Hall (SRH) recombination model were also used. The bandgap narrowing (BGN) model was taken to consider into account the highly doped regions of the device.

To study the effect of the gate material on the TFET characteristics, HfO_2 and SiO_2 are used as source and drain spacers' materials respectively, but the gate material will be variable. Ge, InAs and Si are used as source materials. Fig.3 (a) and (b) illustrates the drain currents and the total capacitances versus gate voltages respectively.



(a)

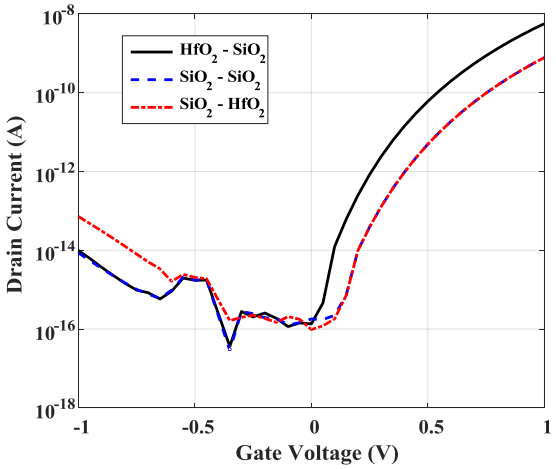


(b)

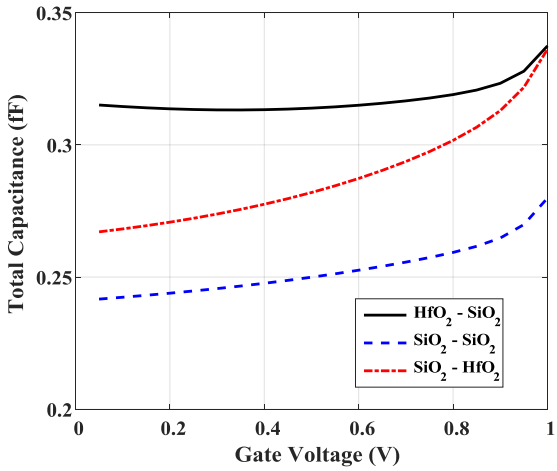
Fig. 3 Effect of source material (a) Drain current vs. gate voltage and (b) Total capacitance vs. gate voltage

From the Figure, it is clear that InAs gives the higher ON current and higher OFF current and also the higher total capacitance. Ge gives high ON current and the less OFF current and medium total capacitance. Si gives the less ON current and less total capacitance. So germanium is preferable to be used as a source material as it gives best characteristics.

Fig. 4 shows the effect of spacers' materials. The figure illustrates the drain currents (Fig. 4(a)) and the gate-gate capacitances versus gate voltages (Fig. 4(a)) where the gate material is germanium but the source and drain spacers are variable. There are three cases, in the first case both source and drain spacer are SiO_2. In the second case, the source spacer is HfO_2 and the drain spacer is SiO_2. In the third case, the source spacer is SiO_2 and the drain spacer is HfO_2. From the curves, it can be seen that the second case gives the highest ON current but it also gives the highest gate-gate capacitance.



(a)



(b)

Fig. 4 Effect of spacers' materials (a) Drain current vs. gate voltage and (b) Total capacitance vs. gate voltage

To study the high-frequency performance due to the effect of the spacers, the cut-off frequency is extracted from the AC analysis. So, the high-frequency figure of merit is analyzed in terms of the unit-gain cut-off frequency (f_T) which is calculated as:

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{GG}} \tag{2}$$

Where C_{GG} is the overall gate capacitance. Fig. 5 shows a comparison between the different types of spacers' materials. Based on this comparison, it can be concluded that using HfO_2-SiO_2 as spacers is most advantageous in terms the high-frequency performance.

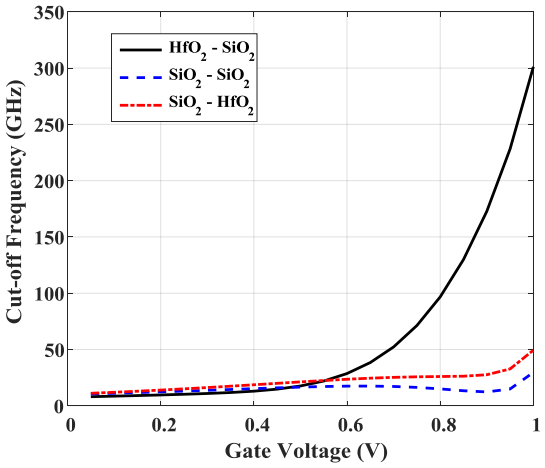
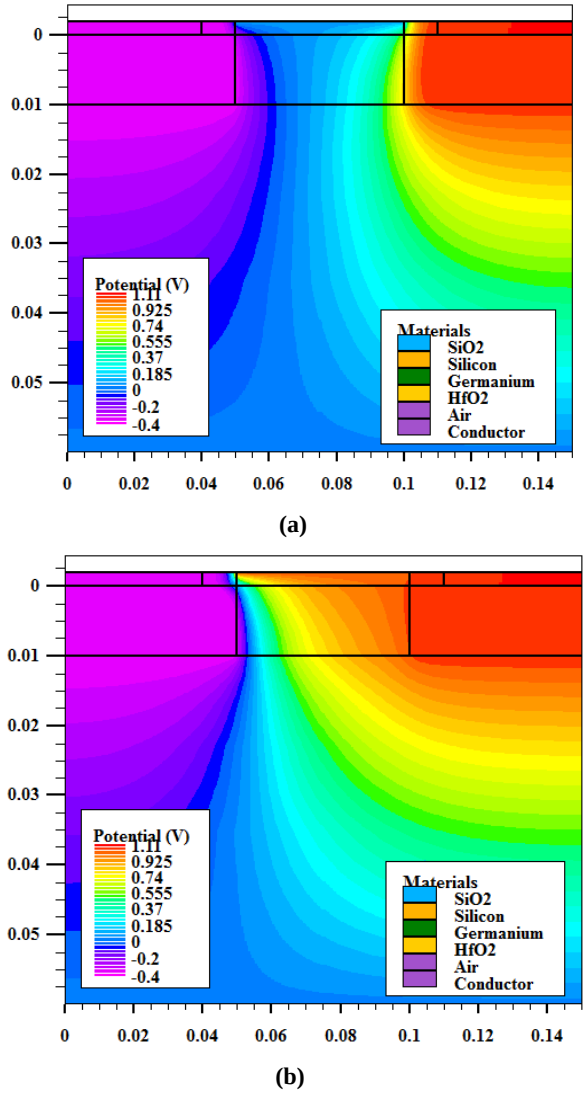


Fig. 5 Cut-off frequency vs. gate voltage



(a)

(b)

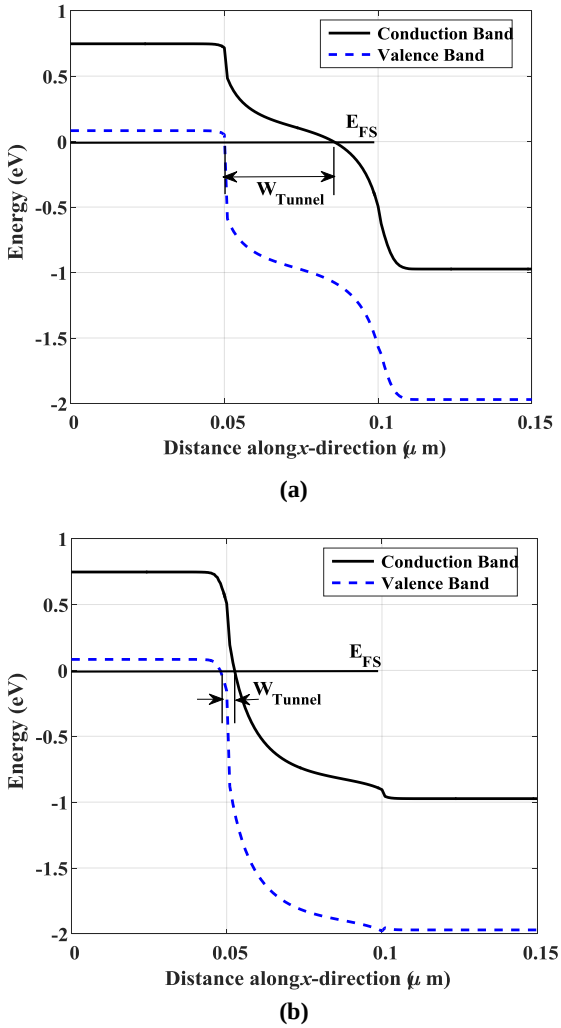
Fig. 6 Potential distribution (a) at V_{GS} = 0, and

(b) at V_{GS} = 1 V

It is evident from the previous simulation results that it is most proper to use Ge as a source material and HfO_2 as a spacer over the source and SiO_2 as a spacer over the drain. In the following simulations, this specific case is considered.

The electrical potential contours in the device structure are shown in Fig. 6 for the OFF state (Fig. 6(a)) and the ON state (Fig. 6(b)). For the OFF state, the maximum variation can be seen near the drain through the channel. Whereas, for the ON state, the maximum variation in the potential can be seen at the p+-n interface, where the tunneling mechanism is prevailing. The potential variation is responsible for the tunneling of carriers from p+ region to n + region through the nearly intrinsic p-type channel region.

The energy band diagrams in both cases; OFF and On states are shown in Fig. 7. It can be depicted form the figure that when in the OFF state (Fig. 7(a)), the tunneling width of the carriers is very long compared to the tunneling width in the ON state (Fig. 7(a)). This ensures the results presented earlier concerning high ON current and low OFF current.



(a)

(b)

Fig. 7 Energy band diagram in (a) OFF state, and (b) ON state

4. CONCLUSION

In this paper, some techniques to enhance the performance of the TFET devices are studied. In the first technique, different oxide materials for the spacers over the drain and source are used. The chosen materials that give the best performance are HfO_2 as the spacer over the source and SiO_2 over the drain. The second technique is to select a different material of the source other than Si. It is shown that using Ge as a source material provides the best performance. The study is based on

the DC I_D-V_{GS} characteristics as well as the high-frequency characteristics regarding the capacitance and cut-off frequency. In the future work, it is intended to study more materials for the source that may give higher ON current. Also, more dielectric materials with different dielectric constants could be explored especially over the drain and see this effect on the ambipolar current as well as on the cut-off frequency. Taking the nonlocal band-to-band tunneling is also one of the physical models that could be used instead of the Kane model used in this paper.

5. REFERENCES

[1] Sakurai T., "Perspectives of low power VLSI's," *IEICE Trans. Electron*, E87-C, pp. 429–436, IEICE, 2004.

[2] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011.

[3] Sze, S. M., *Physics of Semiconductor Devices*, 1st edn (John Wiley), 1969.

[4] Lundstrom, M. S., "The MOSFET revisited: device physics and modeling at the nanoscale," *Proc. IEEE Int. SOI Conf.* 1–3, IEEE, 2006.

[5] Boucart, K. & Ionescu, A. M., "Length scaling of the double gate tunnel FET with a high-κ gate dielectric," *Solid State Electron.* **51,** pp. 1500–1507, 2007.

[6] Seabaugh, A. C.; Zhang, Q., "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," Proceedings of the IEEE 98 (12): pp. 2095–2110, (2010)

[7] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Performance comparison between p-i-n tunneling transistors and conventional MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 456–465, Mar. 2007.

[8] S. Saurabh and M. J. Kumar, "Impact of strain on drain current and threshold voltage of nanoscale double gate tunnel field effect transistor (TFET): Theoretical investigation and analysis," *Jpn. J. Appl. Phys.*, vol. 48, Article ID 064503, Jun. 2009.

[9] R. Vishnoi and M. J. Kumar, "A Pseudo 2D-analytical Model of Dual Material Gate All-Around Nanowire Tunneling FET," *IEEE Trans. Electron Devices*, Vol.61, pp. 2264-2270, July 2014.

[10] D. B. Abdi and M. J. Kumar, "In-built N+ pocket p-n-p-n tunnel field effect transistor", *IEEE Electron Device Lett.*, Vol.35, No.12, pp. 1170- 1172, December 2014.

[11] T. Krishnamohan, D. Kim, S. Raghunathan, and K. C. Saraswat, "Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive currents and <60 mV/dec subthreshold slope," in *Proc. IEDM Tech. Dig.*, San Francisco, CA, USA, pp. 947–949, 2008.

[12] A. Hraziia, A. Gupta, A. Vladimirescu, A. Amara, and C. Anghel, "30- nm Tunnel FET with improved performance and reduced ambipolar current,", *IEEE Trans. Electron Devices*, vol. 58, pp. 1649–1654, Jun. 2011.

[13]J. Wana, C. L. Royer, A. Zaslavsky, S. Cristoloveanu,"Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling", *Solid-State Electron.*, vol. 65, pp. 226-233, Nov. 2011.

[14] D. B. Abdi and M. J. Kumar, "Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain," *IEEE J. Electron Devices Soc.*, vol. 2, no. 6, pp. 187–190, Nov. 2014.

[15] Shubham Sahay and M. Jagadesh Kumar, "Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using hetero-dielectric box," *IEEE Transactions on Electron Devices*, Vol.62, no.11, pp.3882 - 3886, November 2015.

[16] *ATLAS Device Simulation Software*, Silvaco, Santa Clara, CA, USA, 2015.

[17] W. G. Vandenberghe et al., "Analytical Model for a Tunnel Field-Effect Transistor," MELECON - The 14th IEEE Mediterranean Electrotechnical Conference, pp. 923 – 928, 2008.

[18] Rajat Vishnoi and M. Jagadesh Kumar, "A Pseudo 2D-analytical Model of Dual Material Gate All-Around Nanowire Tunneling FET", IEEE Trans. on Electron Devices, Vol.61, pp.2264-2270, July 2014.

[19] J. Wan, C. L. Royer, A. Zaslavsky and S. Cristoloveanu, "A tunnelling field effect transistor model combining interband tunneling with channel transport", *J. Appl. Phys.*, Vol. 110, No. 10, pp. 104503 - 104503–7, 2011.

6. AUTHOR PROFILE

Gihan.T. Sayah is Assistant Professor, Electronic Engineering Department, Exploration Division, Nuclear Material Authority, Cairo, Egypt. She received PhD and MSc from Ain Shams University, Faculty of Engineering, Engineering Electronic and Communication Engineering Department, Cairo, Egypt. Her area of interest is Simulation and modeling of semiconductor power devices, photovoltaic and radiation detectors.