Robust Design of a Dual Edge Triggered Flip Flop at Low Power for High Speed Applications

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ABSTRACT
The logic construction of a double-edge-triggered (DET) flip-flop, which can receive input signal at two levels of the clock, is analyzed and a new circuit design of CMOS DET flip-flop is proposed. Simulation using SPICE and a 1 micron technology shows that this DET flip-flop has ideal logic functionality, a simpler structure, lower delay time and higher maximum data rate compared to other existing CMOS DET flip flops. By simulating and comparing the proposed DET flip-flop with the other designs present, it is shown that the proposed DET flip-flop reduces power dissipation while keeping the same date rate and can be used for high speed applications.

Keywords
Counter, Hold time, Finite State Machine, Registers Storage Element.

1. INTRODUCTION
In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed in VLSI design.[1] One of the primary driving factors has been the remarkable success and growth of the class of wireless communications systems (personal digital assistants and personal communicators) which demand high-speed and complex functionality with low power consumption.

In a digital system, synchronization/clocking has its special role. By its action as timing signal the system clock controls the working rhythm of the chip. If the system is considered as a set of interconnected gates and flip-flops, the clock signal controls all flip-flops to sample and store their input data synchronously. Therefore, the clock signal tends to be highly loaded. In addition, to distribute the clock and control the clock skew, one needs to construct a clock network (often a clock tree) with clock buffers. All of this adds to the capacitance of the clock net which also happens to have the largest activity (2 transitions per cycles) in a synchronous circuit (ignoring possible hazard activity on same signal lines). Recent studies indicate that the clock signals in digital computers consume a large (15% - 45%) percentage of the system power.[2] Thus, reducing power dissipation due to the clock net is an important task in LSI designs, such as the wireless communication system.

Power consumption and energy efficiency plays a vital role in sequential circuit design. Clock gating is a technique that is used to reduce the dynamic power consumption of idle modules. Usage of Dual Edge Triggered Flip-flop (DETFF) is an efficient technique since it consumes half the clock frequency and less power than Single Edge Triggered Flipflops (SETFF's). Integrating clock gating technique with DETFF reduces the power consumption further.

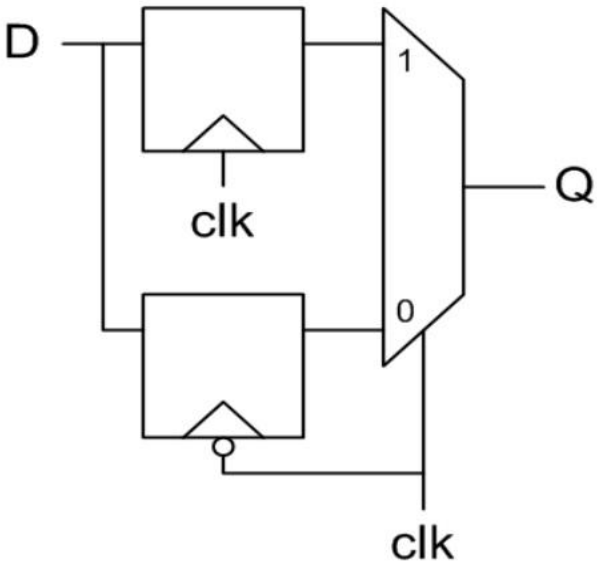

Fig 1. A Simple DET-FF Design

Dual edge triggered flipflop (DETFF) reduce clock frequency at half of the single edged triggered flip-flop (SETFF) with same data throughput therefore it gives better performance in terms of power.

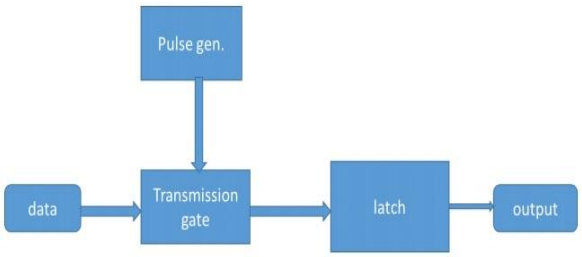

Fig 2. Block Diagram for a DET-FF

2. CONVENTIONAL DET-FF
Figure 3 shows a conventional design of a dual edge triggered flip flop (DETFF). If each inverter have τi sec propagation delay then input clock pulse is skewed by 4τisec that is signal y, and signal x is inverted form of input clock pulse having delay of 3τisec.

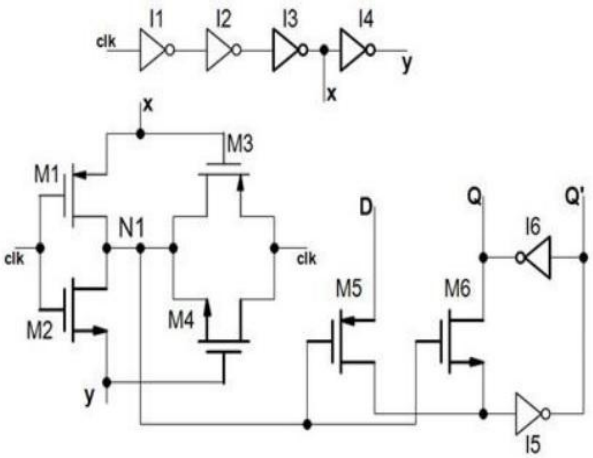

Fig 3. Conventional DET-FF

Inverter shown in bold have higher threshold voltage. MOS M1, M2, M3, M4 are connected such that node N1 = clk Θ y, this is shown in Fig.4. When clk transit from 0 to 1, M2 goes ON (M1 goes off, M3 will ON after 3τi sec and M4 will ON after 4τi sec) and N1 discharged through M2 for 4τi sec since signal y = clk(t-4τi), after 4τi sec N1 charged through M1 and M4. And when clk transit from 1 to 0, M1 goes ON (M2 goes off, M3 will off after 3τi sec, M4 will off after 4τi sec) and N1 discharged through M1 and M3 and M4 for 4τi sec (mostly discharged through M4), after 4τi sec N1 charged through M2 and M3. It is well known that nMOS (pMOS) is bad 1 transmitter and good 0 transmitter (bad 0 transmitter and good 1 transmitter). This is why, combination of M1, M2, M3, M4 used to provide good stability to logic levels. Thus N1 provides XNOR between clk and y.

Input D is connected to M5. When N1 is at logic 0 (for 4τi sec), D is getting transferred to output Q through M5, I5 and I6. And when N1 is at high logic, M5 goes off and M6 turns ON thereby output Q get latched.

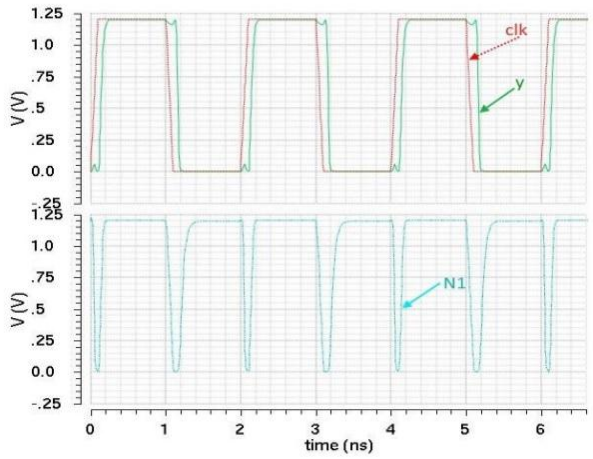

Fig 4. N1 = clk Θ y

3. PROPOSED DET-FF (2)

Proposed_2 DETFF is little modification in conventional DETFF. Fig.5 shows its schematic. Proposed_2 DETFF utilizes transmission gate to pass the data to latch stage.

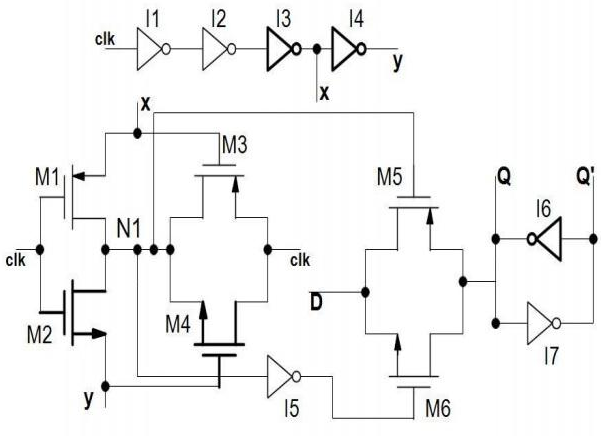

Fig 5 Proposed_2 DETFF

To active both MOS (M5 and M6) in transmission gate simultaneously inverter I5 is used. Here latching of data do not depend on level of N1. D is transfer to Q, when N1 is at logic 0 otherwise change in D do not affect output Q.

4. PROPOSED DET-FF (1)

To generate sharp pulse from clock, a XOR logic is utilized in Proposed_1 DETFF. In this, I1, I2, I3, I4 is used to shift the clock by 4τi sec where τi is delay provided by single inverter. Fig.6 shows schematic of Propsed_1 DETFF.

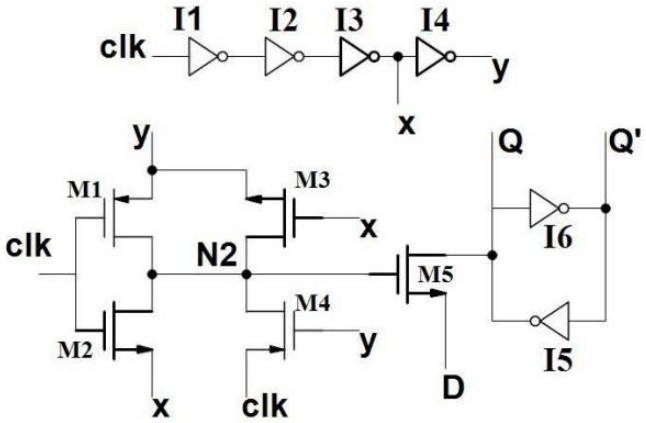

Fig 6 Proposed_1 DETFF

Here y = clk(t-4τi) and x = clk'(t-3τi). When clk transit 0◊1, M2 goes ON, M1 goes off, M3 goes off after 3τi sec and M4 goes off after 4τi sec. N2 get charged through M4 for 4τi sec, however M2 also help to charge N2 for 3τi sec. And when clk remains at 1, then M2 ON, M1 off, M3 off, M4 off thereby N2 get discharged through M2. When clk transit 1◊0, M1 goes ON, M2 goes off, M3 goes ON after 3τi sec, M4 goes ON after 4τi sec therefore N2 get charged through M1 for 4τi sec. And when clk remains at 0 then N2 discharged through M1, M3, and M4 quickly. Thus at N2 a sharp logic high level (for 4τi sec) produced whenever there is transition in clk pulse otherwise N2 remains at logic zero. Hence N2 = clk ⊕ y. Pictorial view of signal at N2 shown in Fig.7.

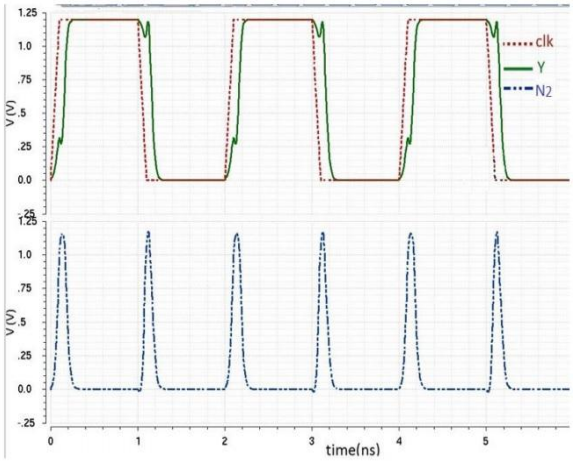

Fig 7 Output from node N2

M5 get triggered when N2 is al logic 1 and data D get latched by I5 and I6. Note that when clk do not change its logic state, change in D do not affect output Q.

5. SIMULATION RESULTS

The proposed DETFFs and DETFF in [1] were designed using gpdk 90nm CMOS technology and simulated by SPECTERE program. All simulation done at room temperature (300K) after considering RC effect of layout (known as post-layout simulation) for different supply voltages and different clock frequencies at fix data pattern. Comparison of simulated result are summarized in Table 1. Set-up time and hold time of DETFFs were found by method as described in [2]. Different type of simulation waveforms (i.e. power vs. supply voltage, delay vs. supply voltage, power vs. frequency and PDP vs. supply voltage) also shown in Fig.8

Table 1 Comparison of DETFFs

Circuit used	Clock Freq. (MHz)	Power Supply (V)	tpd delay (ps)	Power (µW)	PDP (fJ)	t_{su} (ps)	t_{hl} (ps)
Conventional DETFF [3]	500	1.2	85.45	15.7	1.34	-2	150
	500	1.5	66.46	26.23	1.74		
	500	2	52.78	54.54	2.87		
Proposed_1 DETFF	500	1.2	76.52	16.84	1.34	20	75
	500	1.5	53.61	28.7	1.53		
	500	2	47.64	61.29	2.91		
Proposed_2 DETFF	500	1.2	61.93	15.46	0.95		
	500	1.5	48.17	26	1.27		
	500	2	34.62	54.32	1.87		

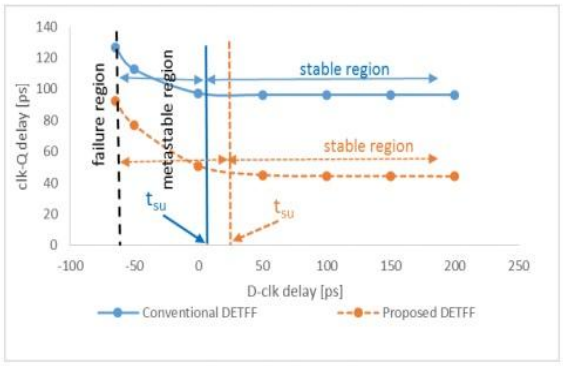

Fig 8. Metastable, stable and failure zone

Proposed DET-FF consumes more power since it have more number of transistor thereby have more area but have less propagation delay as compared to conventional DETFF shown in Fig.5 because it don't have extra an MOS to latch the output unlike conventional DETFF.

Propagation delay is the delay between latching edge of clk to corresponding edge of Q. Here four types of conditions can be generated between clock to output Q, one is Q can be rise at falling edged of clock, second is Q can be fall at falling edge of clock, third is Q can be rise at rising edge of clock and fourth is Q can be fall at rising edge of clock. Finally propagation delay is calculated by taking average of delays for these four conditions. Setup time and Hold time also described in Table 1.

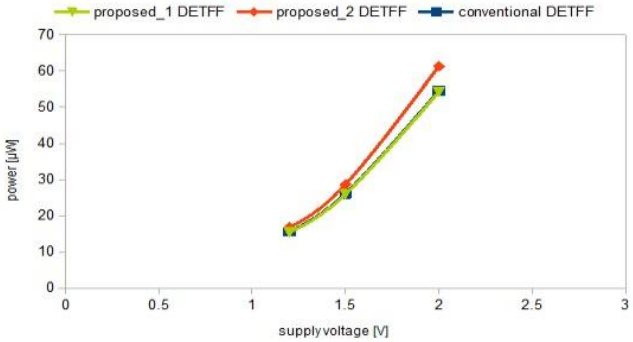

Fig 9. Power vs Supply Voltage curve

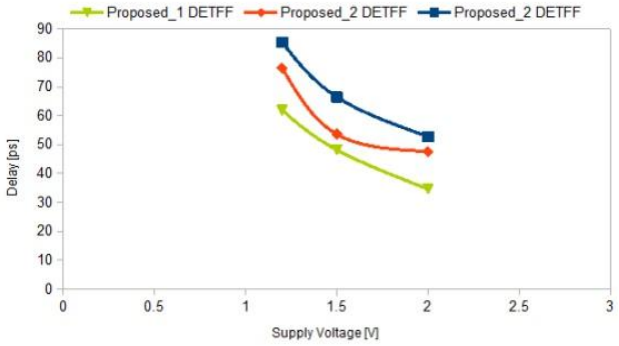

Fig 10. Delay vs Supply Voltage

6. CONCLUSION

Two design of DETFF for low PDP were proposed in this paper. Proposed_1 DETFF uses pass transistor to transmit data whereas Proposed_2 DETFF uses transmission gate to do the same. In Proposed_2 DETFF, to transfer data through transmission gate one extra inverter has been used this increase area of layout as well as power consumption. Proposed_1 DETFF consumed nearly equivalent power to conventional DETFF but work fast thereby overall PDP has been reduced. In case of proposed_2 DETFF to which consumed more power than conventional DETFF, but have less propagation delay. It shows considerable improvement in PDP only at 1.5 V supply voltage. In view of PDP Proposed_1 DETFF and Proposed_2 DETFF outperform conventional DETFF by 29% and 12 % at 1.5 V supply voltage respectively.

7. REFERENCES

[1] W.M. Chung, T. Lo, and M. Sachdev, "A comparative analysis of low-power low voltage dual-edge-triggered flip-flops," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014 (accepted).

[2] A.G.M. Strollo and D. De Caro, "Low Power Flip-Flop with Clock Gating on Master and Slave Latches," Electronics Letters, vol. 31, no. 4, pp. 294-0295, February 2012

[3] A. Gago, R. Escano, and J.A. Hidalgo, "Reduced Implementation of D-type DET Flip-Flops," IEEE J. of Solid-State Circuits, pp. 400-442, March 2011.

[4] R.P. Llopis and M. Sachdev, "Low Power, Testable Dual Edge Triggered Flip-Flops," 1996 International Symposium on Low Power Electronics and Design, pp. 341-345, 2011.

[5] M. Pedram, Q. Wu, and X. Wu, "A New Design of Double Edge Triggered FlipFlops," 1998 Proceedings of the Asian and South Pacific Design Automation Conference (ASPDAC'98), pp. 417-421, 1998.

[6] A.G.M. Strollo, E. Napoli, and C. Cimino, "Low Power Double Edge-Triggered FlipFlop Using One Latch," Electronics Letters, vol. 35, no. 3, pp. 187-188, 1999.

[7] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, and M. Sachdev, "Comparative Delay and Energy of Single Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops for High-Performance Microprocessors," 2001 Symposium on VLSI Circuits, Digest of Technical Papers., pp. 217-218, 2010.

[8] T.A. Johnson and I.S. Kourtev, "A Single Latch, High Speed Double-Edge Triggered Flip-Flop (DETFF)," The 8th IEEE International Conference on Electronics, Circuits and Systems, 2001, vol. 1, pp. 189-192, 2001.