Design and Analysis of Transient Fault Tolerance in SRAM with different NT Techniques

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ABSTRACT
In digital domain applications one of the main important analyses is to check the system performance even if the fault is occurred. This paper describes the fault tolerance technique based on the software approach for SRAM memory unit present in the multi core system using Processor Level Redundancy (PLR). The PLR proceeds with software-centric approach, soft fault tolerance which ensuring a correct software execution. In this approach we applied here only for SRAM available in the processor. The scheme is used at user space level which does not necessitate changes to the original application. In this approach is used to detect the soft errors presented in the memory unit and it will recover from the fault without stop the process of the memory unit. To design the SRAM here we use the different nT technique. The main goal of this approach is which implements fault error detection and fault recovery mechanism to check the performance of the memory unit. This paper presents software based nT for SRAM design and analysis transient fault tolerance using Process Level Redundancy (PLR) is lower when comparable to existed.

Keywords
SRAM, Fault Tolerance, Process Level Redundancy, nT design

1. INTRODUCTION
Transient faults, also called as soft errors, which concern in the reliability of computer systems [1]. A transient fault occurs even in the presence of error. Fault cause error results failure. Fault cause error observed by deviation from expected behavior results failure. It occurs event (e.g., cosmic, device coupling) alleviation or removal of sufficient charge to invert or change the state of the transistor. The inverted value may show effect on program under execution. Current trend in process technology shows that the error rate will remain comparatively constant in future [2]. The number of usable transistor per chip continuously grows in an exponential manner, which increases dramatically. These trends had shown that to ensure correct execution operation of systems. Transient fault characteristics are availability, accessibility, dependability and reliability. The memory is easily protected with error correcting code and parity within high performance microprocessor [3]. However, the same specified techniques cannot be adopted for general purpose computing domain directly.

Application specific constraints Fault results in a glitch which user may not be noticed. Then, the reliability improves to meet user requirements of failure rates. While software technique cannot render a reliability level of hardware technique, they significantly provides a low cost and flexible (zero hardware design cost).existing software transient fault tolerance approaches use the encyclopedias to insert redundant instructions for checking computation and control flow process. Redundant more than is needed, desired or required to ensure correct execution [4].

2. LITERATURE SURVEY
Recent work has demonstrated the use of transient fault which describes the service even in the presence of fault. It describes a low overhead software based approach [5-6]. Fault can be classified by benign fault, Silent Data Corruption (SDC) and Detected Uncoverable Error (DUE) [7]. Benign fault is a transient fault that does not propagate to affect the correctness of an application. Many benign faults that propagate without affecting program correctness can be safely ignored [8]. A transient fault that is undetected and propagates to corrupt program output is considered as Silent Data Corruption SDC. Detected Uncoverable Error (DUE). A transient fault which is detected and propagates without possibility of recovery is considered a DUE.

![Figure 1](image)

(a) Hardware-Centric (b) Software Centric

Figure 1. Hardware and Software-Centric Transient Fault Detection Models

Most previous access is hardware-centric-even compiler approaches. Swift software implemented fault tolerance technique is used. Software Centric is able to leverage the strength of a software approach. PLR improves performance over existing software transient fault tolerance techniques and moves ahead to make it possible for software fault tolerant solutions with comparable performance to hard-ware techniques [9-10]. In Fig.1, Transient fault provide a service even in the presence of error. Fault causes error results in failure.SOR concept are used for defining the boundary of reliability in redundant hardware design [11-13].

3. METHODOLOGY
Many problems become increasingly large and complex, forcing the use of digital system design for their efficient and effective applications [14-15]. Here the circuit design consists of SRAM block, shift register, adder, and master and slave process. Top module consist SRAM which is used to store the data. Shift register we used totally are three shift register, they are group of flip flops cascaded in chain. All the flip flops are driven by a common clock. Next stage is master and slave
process we are designing adder circuit. Watch dog timer which is used to detect the error here designed as a NOR and inverter.

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The schematic design Fig 2 is shown below with three redundant processes. Thus, the reliability improves to meet user expectations of failure rates. This is mainly used to leverage overhead mechanism.

Now we are designing memory in that memory design input signal are given to memory to store the memory value with respect to word line WL. If WL high mean the data will be positive in shift register module or else it will be store as it is. Shift register consists of D flip flop with five bit. Based on input memory will produce the output with respect to clock signal. From the output of shift register is given to master and slave module it will function the full adder. Full adder process designed by using a two half adder.

SRAM reveal data reminisce, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. Static memory which is mainly used for a storage device it is a permanent storage. Shift register are sequential logic circuit used for storing binary digits. They are group of flip-flops connected in a chain. So that the output received from one flip-flop becomes the input of next flip-flop. A common clock drives all the flip-flops and all are set or reset simultaneously. One of the redundant processes assigned to be the master process and the other one as the slave processes. Here we used a adder application here two half adder as designed as a full adder which propagates the sum and carry output. Modeling of the memories is needed to optimize power, delay and area in SRAM design and to characterize the behavior of the SRAM and help making design decisions before running SPICE simulations. There have been many proposed models and tools developed to predict the SRAM performance. However, these models and tools are all based on traditional 6T, 6.5T, 8T and 10T SRAM design.

4. RESULTS AND DISCUSSIONS

4.1 Shift Register
In Fig.3, shift register are a type of sequential logic circuit mainly used for storage. They are group of flip-flops connected in a chain. So that, the output received from one flip-flop becomes the input of the next flip-flop. All the flip-flops are driven by common clock and all are set or reset simultaneously. SISO are connected in a chain one of the flipflop output becomes the input to the next flip flop which are driven in a common clock. it is mainly used for the storage device consists of number of register.
4.4 6.5T SRAM CELL

The basic architecture of the proposed write read decoupled SRAM block illustrated in Fig. 8. The number of transistors in each block depends on the number of bits stored in the block. The average-6.5T block holds sixteen bits through sixteen back-to-back connected inverters the storage nodes are connected to the local bit-lines (LBL and LBLB). These local bit-lines are decoupled from the write bit-lines (WBL and WBLB) via Mwr1–2 during a write operation and from the global read bit-lines (RBL and RBLB) via Mrd1–4 during a read operation. This new write/read-decoupled (WRD) technique allows complete isolation of these sixteen bits. The schematic consists of 6.5T SRAM and the average-6.5T block holds sixteen bits through sixteen back-to-back connected inverters, shift register, and adder master and slave process. The simulated output of fault free and faulty outputs are shown in Fig. 9 and 10.

4.5 Base Full 8T SRAM Schematic

The design of an 8T SRAM cell (Shown in Fig.11), at the start of the read cycle the read bit line is pre charged to full swing voltage. After the pre charge phase is over, Read Word line (RWL) is asserted that drives the access transistor M5 ON. The schematic is based on the structure of 8T SRAM based base full schematic which consist of memory block, shift register, redundant process of master and slave process. The simulated output of fault free and faulty outputs are shown in Fig. 12 and 13.
4.6 10t Sram Base Full Schematic

In Fig.14, 10T SRAM is similar to the 8T SRAM with extra transistors are connected to the read decoupled path with bit lines (BL & BLB) to avoid the draining of read current to ground. The architecture of the 10T cell is similar to the single ended 8T cell. In addition to the 8 transistors, 2 transistors are added in the decoupled read path. The simulated output of fault free and faulty outputs are shown in Fig. 15 and 16.

4.7 POWER ANALYSIS AND OPTIMIZATION

From this power result we also calculate the Power Delay Product ((PDP=average power consumed * propagation time delay), in fJ (10^-15))

\[ \text{Static current} = \frac{I}{V} \text{ (mA)} \]

Operating frequency=\( \frac{1}{T} \text{ HZ} = \frac{1}{T_{\text{on}}+T_{\text{off}}} \)

To calculate the Area of Transistor:

Area of transistor=No. of transistor*length * width (\( \mu \text{m}^2 \))

Throughput=operating frequency*No. of bits at output (bits/sec)

SRAM is semiconductor memory cell. It stores one bit of information. It is faster and consumes very less power as compared to other memory cells. SRAM is vital component in a chip or microprocessor IC. 10T SRAM cell performs better than 6T. The following comparison Table 1 shows that the detail about the design of 6T,6.5T,8T and 10T. The optimization is based on the simulation results of 6T,6.5T, 8T ,10T of average power consumed power and delay we calculate the following table from this we optimize the how power consumed and concluded that the 10 T SRAM has advantageous compared to 6T and 8T. The total base full schematic consumed the average power,static power,static current,energy delay product be optimized in Table 1 shows that the four parameters comparative study for 6T,6.5T,8T and 10T.
μw- Micro Watt , mw- milli watt , mA- milli Amperhem , nws-newton watt second

Table 2: Power Delay Product

<table>
<thead>
<tr>
<th>Parameters</th>
<th>6T</th>
<th>6.5T</th>
<th>8T</th>
<th>10T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power average</td>
<td>0.177mw</td>
<td>2.126mw</td>
<td>0.222mw</td>
<td>0.109mw</td>
</tr>
<tr>
<td>Static power</td>
<td>11mw</td>
<td>63.4mw</td>
<td>16mw</td>
<td>8.63mw</td>
</tr>
<tr>
<td>Static current</td>
<td>6.1mA</td>
<td>35.22mA</td>
<td>8.8Mα</td>
<td>4.7Mα</td>
</tr>
<tr>
<td>Energy Delay Product</td>
<td>1.9278mws</td>
<td>289.60ws</td>
<td>1.6070ws</td>
<td>604.50ws</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>25Hz</td>
<td>25Hz</td>
<td>25Hz</td>
<td>25Hz</td>
</tr>
<tr>
<td>Area of transistor</td>
<td>3.75μm²</td>
<td>40μm²</td>
<td>5μm²</td>
<td>6.25μm²</td>
</tr>
<tr>
<td>Throughput</td>
<td>25 bits/sec</td>
<td>25 bits/sec</td>
<td>25 bits/sec</td>
<td>25 bits/sec</td>
</tr>
</tbody>
</table>

5. CONCLUSION & FUTURE WORK
To remove all glitch in the circuit and to design a fault free circuit. It can be concluded that focuses on a method of charge sharing between the bit lines of 10T SRAM and these method consumes less power for read operations and cut systems dynamic power budget to greater extent. The significant improvements obtained in the results through the use of 10T cell which will be applicable for future low power memory design. Fault injection demonstrates a known fact that PLR’s software-centric fault detection model detects faults to an acceptable degree by safely ignoring benign faults. Present a software implemented transient fault tolerance technique to utilize general purpose hardware in SRAM with multi cores. PLR performance meliorates upon existing software transient fault tolerance techniques and takes a step toward enabling software fault tolerant solutions with comparable performance to hard-wire techniques. Applications such as sensor network domain that is battery driven application. In future work we will design a processing unit circuit and study about how to design circuits with multiple outputs.

6. REFERENCES
[1]. Alex Shye, Student Member, IEEE, Joseph Blomstedt, ‘PLR: A Software Approach to Transient Fault Tolerance for Multi core Architectures’ IEEE Transactions on Dependable and Secure Computing (TDSC), April-June 2009 (vol.6 no.2) pp. 135-148.


