Study of Parasitic Effects of 1st Generation in 4T Relay Design

Soumitra S. Pande
Scholar, EC Department
AISECT University
Bhopal (M.P.)

Sanjiv Gupta
Professor & Head
Department of Electronics & Communication Engineering
AISECT University, Bhopal (M.P.)

ABSTRACT
The novel 4T Design(1), though efficient, has several parasitic effects of 1st Generation accumulated in it. These parasitic effects are discussed in this paper. After testing the prototype, it was observed that effects like body effect, drain actuation etc. are still present in the system. This paper discussed them all and provides a key to solve the issues rising from these effects.

Keywords
Body effect, drain actuation, Novel, parasitic, prototype

1. INTRODUCTION
In (1), a new flexible 4T Relay design was discussed. The design was coherent, robust and efficient. Also in the same paper the DC Characteristics of the system was reviewed.

The design has a clamped-clamped structure and four symmetric flexures with dimpled contacts. (Fig 1)

2. PARASITIC EFFECTS OF 1ST GENERATION IN 4T RELAY DESIGN
As stated earlier,(2,3) The design of the first working relay prototype is not perfect. Several undesirable phenomena were observed during device and circuit testing. Figure 2 shows the areas of the electrodes and the associated capacitances between them that exist in this relay design.
contributes to electrostatic force \( C_{\text{ACTUATION}}=C_{GB}=19.5 \) fF, resulting in a much weaker electrostatic force. While the current design necessitates the W electrode to always be smaller than the SiGe electrode to account for the source/drain regions, the area difference can be minimized in an optimally designed relay. (7,9)

### 2.2 Body effect

Figure 4 shows how the switching voltages shift with applied body bias. Ideally, actuation would depend only on the voltage difference between the gate and the body \( V_{\text{GB}} \), so \( V_{\text{PI}} \) and \( V_{\text{RL}} \) should shift the same amount as the applied VB (i.e. slope = 1). However, everywhere a capacitance forms, electrostatic force exists to influence actuation. The slopes seen are instead ~0.5. Out of a total plate area of 810 µm², only about half (450 µm²) forms capacitance with the body electrode (hence the slope of ~0.5). The gate-to-body electrode overlap should be maximized for body biasing to be more effective. (1)

![Fig 4 Dependence of the pull-in voltage (V\text{PI}) and the release voltage (V\text{RL}) on body bias (VB). For a given VG, more negative VB results in larger VGB (larger electrostatic force) and so reduces VPI and VRL, and vice versa.](image)

### 2.3 Parasitic Source/Drain Actuation

Figure 5 shows that the drain and source bias voltages \( V_D \) and \( V_S \) also affect VPI due to parasitic electrostatic forces. Ideally, the source and drain should have minimal effect to the switching voltages (i.e. slope = 0). The gate-to-source/drain overlap area \( A_{GD} + A_{GS} = 300 \) µm² compared to gate-to-body overlap area \( A_{GB} = 450 \) µm² is significant (~2/3). Thus, \( V_{\text{PI}} \) and \( V_{\text{RL}} \) are also influenced by \( V_D \). This is a phenomenon similar to Drain Induced Barrier Lowering (DIBL) in CMOS, which causes \( V_{TH} \) lowering with higher \( V_D \). In an optimal relay design, the source and drain should not overlap with the actuated plate, so that \( A_{GD} \) and \( A_{GS} \) is minimized. (1)

![Fig 5 Dependence of the pull-in voltage (V\text{PI}) and the release voltage (V\text{RL}) on drain bias (V\text{D}), with V\text{DS} = 1V. Parasitic electrostatic force between the gate and the source/drain results in a shift in V\text{PI} and V\text{RL}.](image)

### 2.4 Parasitic Channel Actuation

Another condition that affects the circuit testing is the inability to turn off the relay in situations where both the source and drain are pulled high (1). Take a simple case of a relay-based buffer shown in Figure 6 (a). When the input is high \( V_{IN} = V_{DD} \), the top relay will be on while the bottom relay will be off. The output is pulled up to high \( V_{OUT} = V_{DD} \). Therefore, both source and drain of the top relay is high (at \( V_{DD} \)). In cases such as this, the relay could not be turned off, even after \( V_G \) is lowered back to zero. As illustrated in 6 (b), the channel potential is also at VDD resulting in electrostatic force between the channel and the body (8). A large overlap area between the channel and the body \( A_{CB} \), creates electrostatic force large enough to overpower the spring restoring force \( V_{RL} \) drops to below 0V. In cases where the channel voltage is not high enough to prevent turn off entirely, this phenomenon could still lower \( V_{RL} \) and undesirably increase the hysteresis voltage. Therefore, in a well designed relay, \( A_{CB} \) should be minimized, if not completely eliminated.

![Fig 6 Description of parasitic channel actuation effect observed in the 1st generation 4T relay devices. (a) A buffer relay circuit, one example where this phenomenon can possibly happen. (b) Bias configuration that prevents the device from turning off despite VG lowered back to 0V](image)
3. CONCLUSIONS
The present paper discusses all the parasitic effects which arise while studying the prototype of the Robust 4T Relay design. All these defects are actual defects and arise during the execution period of the design.

4. ACKNOWLEDGEMENTS
The authors would like to thank the teaching staff of EC Department at AISECT University. Also the authors acknowledge the support of Physics and Chemistry Department of Dr. H.S Gour Central University, Sagar (M.P.)

5. REFERENCES


