Abstract

Our computing era has been working long to get a solution for the problem of power dissipation in conventional digital circuitry. Towards this approach, reversible logic has received a significant attention in recent past. Power dissipation occurs due to the loss of information carrying bits during circuit simulation which consequently deteriorates the system performance. Reversible logic allows us to determine the outputs from the inputs and also the inputs can be appropriately recovered from the outputs by using one-to-one mapping. This results in reduced bit loss leading to reduced power dissipation. Reversible logic has been a research paradigm in the field of low-power CMOS, nanotechnology etc. This paper gives a brief description of few reversible logic gates and describes a mathematical derivation to verify how V and V+ gates are square root of NOT gate and Hermitian conjugate of V gate respectively, by using matrix manipulations.

References


**Index Terms**

Computer Science                         Applied Mathematics

**Keywords**

reversible logic, reversible logic gates, NOT gate, V gate, V+ gate