Design of Input Vector Monitoring Concurrent BIST based Architecture for 4-Bit Multiplier

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Abstract

Input vector monitoring in associate with the BIST testing schemes perform testing during the normal operation of the taken circuit without imposing the circuit to be set in offline to perform the test. Testing should authenticate correctness of design and the test procedure. When a new chip is designed and fabricated for the first time, the testing may even take place in the design laboratory rather than in a factory and it frequently needs the participation of the design engineer. IVM-BIST is the best method to perform testing even in offline mode. The proposed method usually used by designers of the systems to check the corrected data received or not. So the fabricated chips first tested before it received by the customer to ensure the quality of the output. This is also known as acceptance testing (or inspection testing) and is conducted either by the user or for the user by some independent testing house. While testing, a part of the circuit (having the fault) is replaced with a corresponding redundant circuit part (by re-adjusting connections), in case any fault is found. BIST is testing a circuit every time before they startup. This paper presents central concepts of testing of VLSI circuits by BIST.
References


Index Terms

Computer Science
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Keywords