Abstract

In wireless communication systems the most important issue to be considered is the ability of the receiver to detect the errors and correct them from the received information, so as to provide correct information data to the processor. A number of different methods are available to implement the hardware and software with such preference. But, when the length of the communication link becomes very long, i.e., the distance between the wireless transmitter and receiver is very large, the effect of noise on the transmitted signal may cause a change in multiple bits of the transmitted information. This can cause drastic loss in many cases. In this brief a Field Programmable Gate Array (FPGA) based design and simulation of Golay Code (G23) and Extended Golay Code (G24) Encoding scheme are presented. This work is based on the optimization of the time delay of the operational circuit to encode a data packet using the Golay Encoder.


High Speed Design of FPGA based Golay Encoder and Decoder


Index Terms

Computer Science Communications

Keywords

Encoder, Decoder, FPGA, Operational Delay