Calculation of Leakage Current in CMOS Circuit Design in DSM Technology

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ABSTRACT
With the continuously growing quest for miniaturization of circuit technology, one of the prime focuses of the research has shifted in the direction of ultra low power circuit designs. As the size of chips is shrinking and the density is increasing simultaneously, losses are increasing mostly in the form of power dissipation. Based on various parameters of performance evaluation in a VLSI circuit and the continuously growing quest for highly efficient and ultra shrunk devices, has compelled the researchers and designers to come up with improved designs which are highly efficient and feasible. In this Paper we have calculate leakage power at different input vector combination with different technology to identify the effect of channel length reduction in CMOS technology. All simulation is performed over on Conventional NAND gate with variation of transistor by using Berkley Predictive Technology Mode at 65nm technology by using HSPICE simulator and analyse in terms Power consumption, delay and PDP with supply voltage of 1V at 100MHz frequency.

Keywords
Low Power, Variation in NAND Gate, CMOS, GIDL, PDP.

1. INTRODUCTION
The rapid advancement in semiconductor technology in electronic devices, over the years has resulted in better performance and higher circuit densities. Astonishing technical advances in semiconductor fabrication, circuit design techniques and computer architecture have enabled an exponential increase in the performance and integration density of microprocessors. As feature size continues to shrink, more number of transistors can be packed into the same chip area, enabling large increases in the transistor count per chip. However, as the size is getting smaller and the integration density increase, the increasing power dissipation has become a primary concern for further development of VLSI circuit technology.

A number of techniques have already been proposed for reducing power dissipation. The two important types of power dissipation in VLSI circuits are 1) Static power dissipation and 2) Dynamic power dissipation. While static power dissipation is due to internal leakages in devices during the off state of a circuit [1], dynamic power dissipation is because of the energy loss during charging and discharging of the output node capacitance of a transistor when switching takes place.

Lately, dynamic power dissipation has been the primary concern of designers. Different technologies have been introduced over the years which are sub-threshold logic [3], multi-threshold logic [4] and static logic circuit [2]. Static logic, which utilizes AC voltage supply as opposed to DC voltage supply so as to recycle the energy of circuits, a promising alternative to CMOS, is a novel low power circuit technology. In contrast to conventional CMOS circuits where energy stored in load capacitors is dissipated to ground, adiabatic logic offers a way to reuse this energy. Combining the ideas of conventional logic with the adiabatic logic circuits together, power dissipation can be reduced drastically [5-7].

This paper has huge potential for reduction of leakage power in section 2 previous research work done so far in the field of Low power technology. It sums up work of different authors which has been published in different journals over the years. Section 3 shows the results and simulation part a comparison is drawn in between all the simulations done to show the effectiveness of different logic families over others. In Section IV drawn conclusions based on the entire work done and from the simulation work and results evaluated

2. LITERATURE SURVEY
2.1 Leakage Power Consumption in CMOS IC
Scaling down of the technology needs to reduce supply voltage due to PD and matter of consistency. However, it requires the reduction of threshold voltage (VTH) of the devices to maintain a reasonable gate overdrive (VDD-VTH) [8], the VTH reduction result in an exponential increase in ISUB, moreover to control Short Channel Effects (SCE) and to maintain the transistor derive strength at low VDD, Oxide thickness (TOX) need to be also scales down. The aggressive scale of TOX result in a high tunneling current over the gate dielectric [8], additionally, scaled devices require the use of the higher substrate doping density. It causes considerably leakage current through these Drain (D) and Source(S) to substrate (B) junction under higher reverse biasing [8-11]. These are the three major contributor of the leakage mechanism: Subthreshold leakage current (ISUB), gate oxide tunneling current (IGATE) and reverse bias PN junction current (IBTBT). In addition to these three major leakage components, there is other ones like Gate Induced Drain Leakage (GIDL) and punch through, those components can be neglected in typical mode of operation.

In DSM technology three domination leakage current occurred in the CMOS device such as ISUB, IGATE, and IBTBT, as shown in Figure 1.

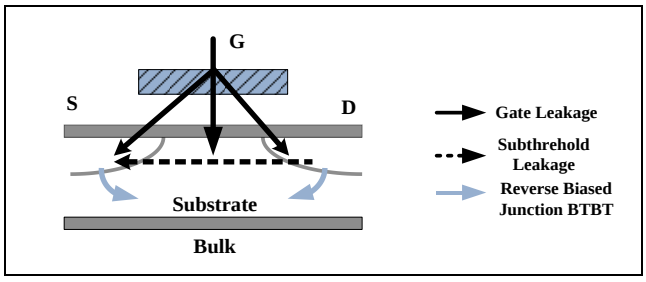


Figure 1. Shows Various Leakage current in DSM technology

2.2 Leakage power dissipation

Total Power dissipation is calculated as:-

$$P_T = P_D + P_{ST} + P_{Short\text{-}circuit} + P_{Static\text{-}DC}$$

Where PT is the dynamic or switching power dissipation, occurs due to charging or discharging the parasitic capacitances in node voltage transition. PST is the static or leakage power dissipation, combination of the subthreshold leakage power due to the not ideal off state. PShort-circuit is the short circuit power dissipation occurs during switching operation when both the Pull Up and Pull Down networks are in ON state. P Static-DC is the static DC power dissipated

The main power contribution is CMOS technology is basically Sub-threshols Leakage and gate oxide leakage current is the dominant in nanometer regime [12-16].

a) Sub-threshols Leakage

Sub-threshold leakage current is very significant component of the leakage power and this current passes from drain to source through the channel [6-7]. The sub-threshold leakage current is caused basically due to carrier diffusion between the source and drain region of the transistor in weak inversion. For a particular MOS transistor whenever applied gate to source voltage is less than the threshold voltage of the transistor, there is no flow of current. Mathematically

When $V_{gs} < V_t$

$I_{ds} = 0$

b) Gate oxide tunnelling current

Tunnelling through gate oxide occurs because thickness of gate oxide layer is gradually reduced as technology is reducing[7]. The gate oxide tunnelling current is caused because of tunnelling of electrons through nMOS capacitor with a heavily doped n+ polysilicon gate and p type substrate .

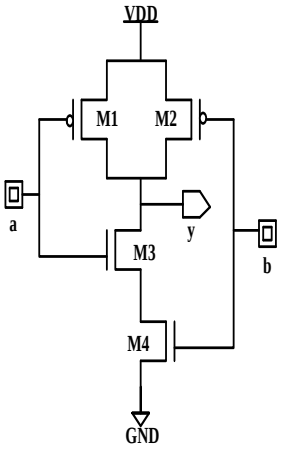


Figure.2. Graphical representation of 2input NAND gate

During operation of two input NAND gate (i.e. input vector '00'), then transistor M1 and M2 turn ON and transistor M3 and M4 turns of in which take part in leakage current. When input vector(i.e. is 01) the transistor M2 and M4 turn off and take part in leakage contribution, at input vector 10 M1 and M3 turns off and take part in leakage current contribution. When input vector is 11 maximum leakage current flows by the two M1 and M2 transistor. These parameters are Leakage Current (ILeak), Static Power dissipation (PST) and Dynamic Power dissipation (PD), Total Power (PT), delay and PDP. Performance of CMOS circuits is depends on these parameters.

For DSM circuits mainly ISUB is the dominating component of power dissipation in CMOS IC as shown in Figure.2.

Hence dynamic and short circuit power dissipation are jointly called switching power dissipation. The reasons for static or leakage power dissipation are leakage currents, reverse biased currents and substrate injection currents, which flow through the transistors in its steady states [20-24]. Switching power dissipation arises due to the charging and discharging of output load capacitance during switching. Short- Circuit power dissipation is caused by currents flowing directly from supply to ground for a very short period of time when the p-device is being turned OFF and the n-device is being turned ON during switching.

When the logic 0 is applied at the input terminal of CMOS, NMOS transistor will turn OFF and PMOS will turn ON. As result logic 1 will be available at the output node. When logic 1 is applied at the input, NMOS turns ON and PMOS goes in OFF state, Thus there will be logic 0 at the output node. Power dissipation in CMOS transistors occurs mainly because of the device switching operations. At each charging and discharging operation, there is an inevitable energy loss of CV_{dd}^2 for static CMOS circuits. During charging operation, the energy dissipation through pull-up block from power supply is equal to CV_{dd}^2 , of which half of the energy ($0.5CV_{dd}^2$) is stored in load capacitor. The other half is dissipated through the resistive path, and lost as heat to the environment. Now during the operation of discharging, the residual energy stored in the load capacitor ($0.5CV_{dd}^2$), will be released to the ground through pull-down network

A graph is prepared by nodes and links, which represented by transistors and their interconnection respectively. Figure 2, shows the Graphical representation of 2 input NAND gate. Here a, b are the inputs and y is the output of the given circuit. VDD and GND are the power supply and ground nodes. This logic gate is used as a basic gate for implementation of every other gate for simulation. It is used CMOS logic design style. Here two input NAND logic gate is used as a basic gate for each logic and combinational circuit. Firstly NAND gate and its variants are created using CMOS design style. Secondly all the test circuits are implemented by NAND gate and analyzed by using these variants. it. For Simulation HSPICE is taken as a simulator tool. It requires a spice code (Transistor level net-list) of the desired circuit for their parameters calculation. All the circuits are mapped with 180nm, 130nm, 90nm, 65nm and 45nm BPTM technology file. This file contains every physical design details of a CMOS transistor, where 45nm is the effective length of CMOS transistor. All kind of analysis with mapping of this file is shown through the flow of HSPICE design flow.

3. RESULTS AND SIMULATION

From the simulation we analyse that as we scale town the technologies in deep submicron regime leakage current dominated from Table I. it is observe that when we move form 180nm towards 45nm than leakage current increases drastically upto 94.94% due to reduction of the threshold voltage of CMOS transistor, as we scale down the channel length leakage current increases. Simulation of two inputs Nand is done for all the input vector combination from the Table I. We observe that maximum leakage current flows at 11 input vector combinations at 90nm, 65nm, and 45nm CMOS technology respectively. All the simulation is performed by using BPTM libraries in HSPICE simulator at 180nm, 130nm, 90nm, 65nm and 45nm with load capacitance of 1pF with 10MHz frequent at supply voltage of 1.8V, 1.5V, 1.2V, 1V and 0.9V power

supply to analyse the variation of leakage current with different technology and different supply voltage over smaller channel device. In Table II. We have compared various leakage reduction techniques to develop a new technique for fruit full research.

Table I. Leakage current of 2 Input Nand Gate

Leakage Current (A) for 2 input Nand Gate				
Technology	(0,0)	(0,1)	(1,0)	(1,1)
180nm	6.560p	254.4p	208.3p	41.83u
130nm	36.66p	6.227n	4.874n	15.45n
90nm	88.33p	1.924n	1.593n	4.122n
65nm	167.7p	2.630n	1.975n	2.526n
45nm	129.6p	3.607n	2.239n	4.104u

Average power calculation is done for 2 inputs Nand Gate at different technology we observe that as we scale down the channel length average power also reduces from Table II. We analyse that saving of average power 86.82% with 130nm, 12.25% with 90nm, 17.85% with 65nm at 00 input vector combinations. We also observe that average power consumption is lower at 00 input vector combination and maximum at 11 input vector combinations respectively.

Table II. Average Power consumption of 2 Input NAND Gate

Average Power consumption (µW) for 2 input Nand Gate				
Technology	(0,0)	(0,1)	(1,0)	(1,1)
180nm	7.7867E-12	4.5E-10	3.7E-10	7.5E-05
130nm	1.8075E-09	1.6E-08	7.3E-09	3.7E-08
90nm	2.4134E-10	1.9E-09	1.4E-09	4.1E-09
65nm	2.8421E-10	2.8E-09	1.8E-09	2.7E-09
45nm	2.3829E-10	3.7E-09	2.3E-09	3.7E-06

From Table I and II. we observe the impact of technology scaling and draw the graph leakage current versus technology it is calculated that leakage current increase as we move from 130nm towards 90nm, 65nm and 45nm respectively as shown in Figure.3.

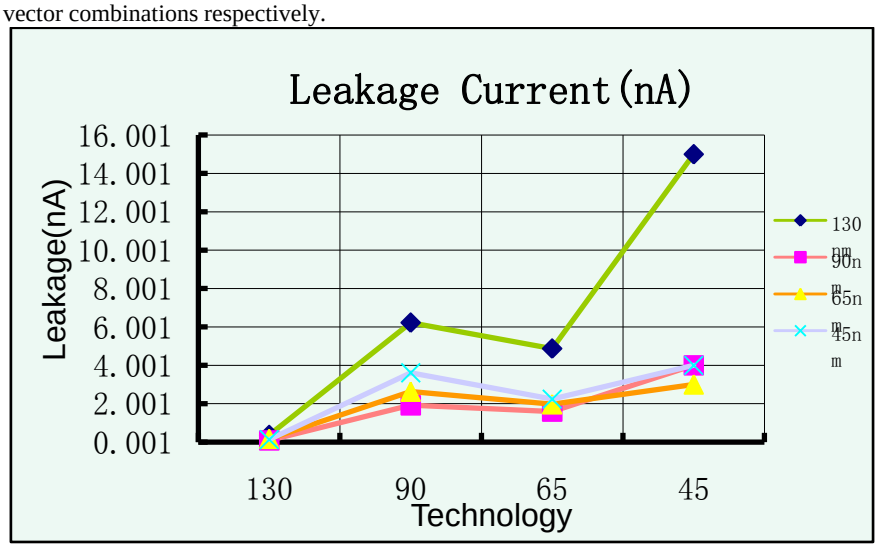
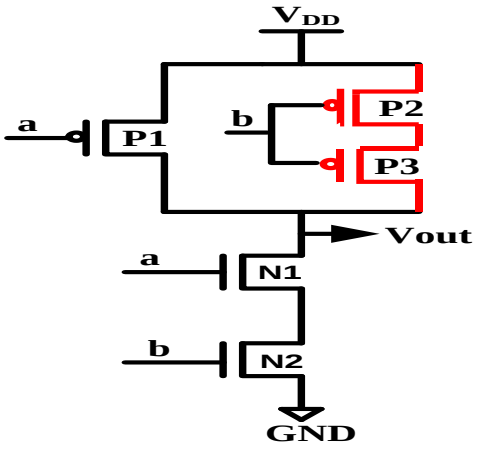
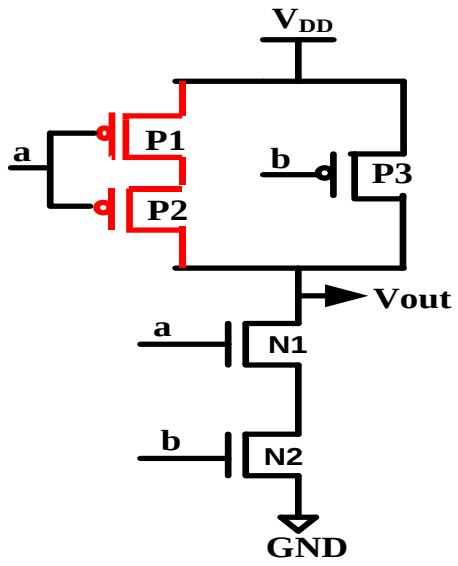


Figure.3. Graph for variation of leakage current with the variation of technology.

Combinational circuit implementation and simulation details are discussed in this chapter. Here two input NAND logic gate is used as a basic gate for each logic and combinational circuit. Firstly NAND gate and its variants are created using CMOS design style. Secondly all the test circuits are implemented by NAND gate and analyzed by using these variants as shown in Figure.4.



(a)



(b)

Figure .4. Variation of two input NAND Gate for Leakage Reduction

For Simulation HSPICE is taken as a simulator tool. It requires a spice code (Transistor level net-list) of the desired circuit for their parameters calculation in Table III.

Table.III. Calculation Two input NAND gate with Variants V1, V2, V3, and V4 results

(i) For Standard NAND Gate				**(ii) NAND Gate with Variation one**			
Input Vector	**I_{Leak} (nA)**	**P_{ST}(nW) + P_{DY} (uW) = P_T(uW)**	**Delay (ps)**	**Input Vector**	**I_{Leak} (nA)**	**P_{ST}(nW) + P_{DY} (uW) = P_T(uW)**	**Delay (ps)**
[00]	**0.49**	**0.57 + .19 = .1906**	**8.13**	**[00]**	**0.49**	**.57 + .17 = .1706**	**8.58**
[01]	**8.24**	**10.5 + .19 = .2005**		**[01]**	**8.24**	**10.5 + .17 = .1805**	
[10]	**2.33**	**2.5 + .19 = .1925**		**[10]**	**2.33**	**2.5 + .17 = .1725**	
[11]	**21.2**	**27 + .19 = .2170**		**[11]**	**10.6**	**15.3 + .17 = .1853**	
(iii) NAND Gate with Variation two				**(iv) NAND Gate with Variation Three**			
Input Vector	**I_{Leak} (nA)**	**P_{ST}(nW) + P_{DY} (uW) = P_T(uW)**	**Delay (ps)**	**Input Vector**	**I_{Leak} (nA)**	**P_{ST}(nW) + P_{DY} (uW) = P_T(uW)**	**Delay (ps)**
[00]	**0.98**	**0.57 + .12 = .1206**	**9.25**	**[00]**	**0.49**	**.57 + .15 = .1506**	**10.3**
[01]	**1.02**	**2.4 + .12 = .1224**		**[01]**	**7.88**	**10.5 + .15 = .1605**	
[10]	**4.59**	**2.5 + .12 = .1225**		**[10]**	**4.59**	**2.5 + .15 = .1525**	
[11]	**0.233**	**3.76 + .12 = .1238**		**[11]**	**0.136**	**3.77 + .15 = .1536**	

Above tables shows results for average power dissipation, delay and power delay product for the conventional NAND From the graphical analysis presented achieves even lesser power dissipation as compared to all other NAND Gate as shown in Table.III. Variation of V1 NAND gate consumes 43.24% lesser power as compared to conventional NAND gate. Variation of V2 gate consumes 39% lesser power as compared to conventional NAND gate. Variation of V3 consumes 29% lesser power as compared to conventional XOR gate and Variation of V4 achieves 35% lesser power.

4. CONCLUSION

The research provides intense focus on leakage current/power analysis and next generation DSM technology. It reflects upon dominating face of leakage power dissipation such as ISUB, IGATE, and IBTBT which are creating higher leakage in DSM VLSI design during idle mode. It proposes a technique for reducing the leakage current during idle mode of circuit. As the quest for ultra-low power circuit designs goes on increasing, these improved circuit technologies would prove to be very useful in serving the need for ultra low power circuit designing. We have compared the results for the least power dissipation achieved using proposed

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