Low Power Combinational and Sequential Circuits with Adiabatic Complementary Pass-Transistor Logic (ACPL)

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ABSTRACT
This paper presents low-power characteristics of adiabatic complementary pass-transistor logic (ACPL) using four-phase AC power supply. Adiabatic CPL circuits consist of pure NMOS transistors, use CPL blocks for evaluation and bootstrapped NMOS switches to eliminate non-adiabatic loss of output loads. In this paper, combinational circuit (4-bit ripple carry adder) and sequential circuit (4-bit binary counter) is realized with adiabatic CPL. These combinational and sequential circuits have been simulated in CADENCE design tool at 90nm technology and simulation results shows that the adiabatic CPL 4-bit ripple carry adder achieve power savings of 80% with PAL-2N logic and adiabatic CPL 4-bit binary counter achieve power savings of 52% with CMOS logic for clock frequencies from 50 to 300 MHz.

Keywords
Adiabatic CPL; Combinational circuits; Sequential circuit; Low-power; VLSI

1. INTRODUCTION
Power dissipation has become a prime constraint in high performance applications, especially in portable and battery operated ASIC systems. With technology scaling, the impact of power dissipation is expected to gain significance. The classical approaches to achieve low-power design are to reduce the supply voltage, the loading capacitances of gates and switching activity [1]. However, these methods have several challenges with the shrink of CMOS technology sizes such as degraded voltage margin, increased leakage currents, and increased soft error rates. Adiabatic logic is a promising alternative low-power approach by utilizing AC voltage supplies (power-clocks) to recycle the energy of circuits instead of being dissipated as heat [2-3].

Previous works on adiabatic circuits achieve considerable energy savings with the help of several adiabatic logic families such as ECRL, 2N-2N2P, and complementary pass-transistor logic (CPAL) [4-7]. Recently adiabatic CPL (an improved design for CPAL circuits) circuits have been presented [8]. In adiabatic CPL circuits, the non-adiabatic energy loss of output loads has been completely eliminated by using complementary pass-transistor logic blocks for evaluation and bootstrapped NMOS switches for driving output loads.

Design of 4-bit ripple carry adder using CPAL [9], 4-bit binary counter using CPAL [10] and Johnson counter using CPAL [11] with four-phase power clocks has been presented.

In this paper, we have designed adiabatic CPL circuits with four-phase power clocks. It consumes less power than other adiabatic logics. We have simulated these circuits at 90nm technology in CADENCE design tool. The simulation results indicate that the adiabatic CPL circuits outperform the other adiabatic circuits in terms of power savings and area requirements.

In section 2, the concept of adiabatic CPL is discussed. Section 3 discusses the circuit topologies for adiabatic combinational and sequential circuits, section 4 presents simulation results and its comparisons.

2. ADIABATIC CPL
The basic structure of adiabatic CPL buffer (inverter) is shown in Fig.1 (a) [8]. It is composed of two main parts: the evaluation logic block and the load driven circuit. The logic evaluation block consists of four NMOS transistors (N1-N4) with complementary pass-transistor logic (CPL). The load driven circuit consists of bootstrapped NMOS transistors (N5 or N6) for driving output loads, so that non-adiabatic loss of output nodes is eliminated. A pair of cross coupled NMOS transistors N7 and N8 is added to obtain non- floating output that makes the un-driven output node grounded. Cascaded adiabatic CPL gates are driven by the four-phase power-clocks as shown in Fig.1 (b). Using the 90nm CMOS process, the simulation waveforms for the adiabatic CPL buffer (Inverter) are illustrated in Fig. 2. These simulation results were obtained when a periodic sequence '101010…' was propagated through the buffer chain. By referring the schematic shown in Fig.1 and the waveforms in Fig. 2, the operation of adiabatic CPL buffer can be summarized as follows.

During the time interval T1, the input IN goes high, while the input INb is low. Therefore, N1 and N3 are turned on; N2 and N4 are turned off. When the input IN is high and N1 is turned on, node A is charged to about (VDD-VTN), where VTN is threshold voltage drop across NMOS transistor. Here node B is clamped to ground due to INb to be low and N3 is turned on.

During T2 the clock (Vclk) goes up and input IN remains at high. As clock charges up the node A can be bootstrapped to a higher level than (VDD-VTN) due to gate-to-channel capacitance of the transistor N5. Therefore, as the clock rises, the node OUT is charged through the bootstrapped NMOS transistor (N5) without non-adiabatic loss. So full swing is obtained at output (OUT). At the same time, when the output (OUT) rises above VTN, N8 will be turned on and the output node (OUTb) is clamped to ground.

During T3, the output (OUT) follows the clock (Vclk), and the node OUTb is still at ground. During the time interval T4, the clock starts falling as the voltage of clock falls from VDD to ground.

The charge output (OUT) node is recovered through the bootstrapped transistor (N5) in the adiabatic manner. From the

above discussion and simulation waveforms, adiabatic CPL hasn't non adiabatic loss on output nodes because its operation for output loads is a full-adiabatic process. Therefore, adiabatic CPL circuits consume less power than other adiabatic circuits.

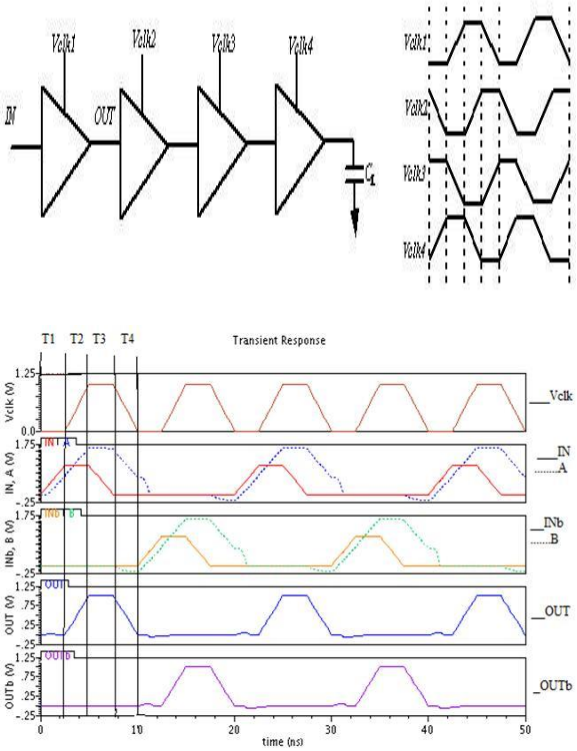


Fig. 1 (a) Adiabatic CPL buffer using four-phase

(b) Buffer chain and power clocks

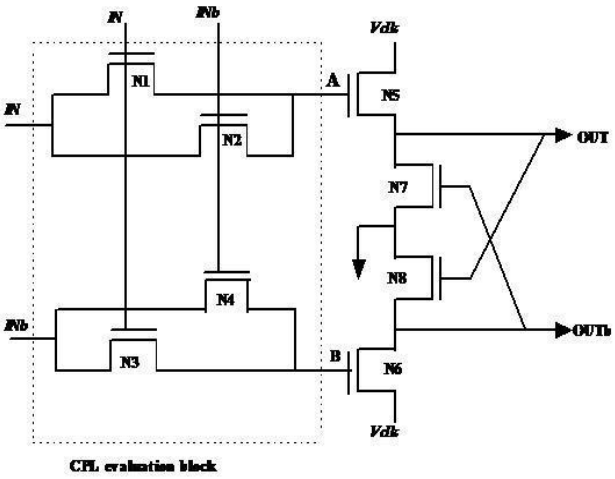


Fig. 2 Simulation waveforms for adiabatic CPL buffer

3. ADIABATIC COMBINATIONAL & SEQUENTIAL CIRCUITS

3.1 4-bit ripple carry adder

The 4-bit ripple carry adder consists of four cascaded full adders [8] shown in Fig. 3(a). The supply for this can be pulse, trapezoidal or sinusoidal signals. Pulses and trapezoidal signals are easy to analyze but difficult to generate hence sinusoidal power clocks are used in all practical purpose which can be generated by simple LC circuits.

For the implementation of 4-bit ripple carry adder , we have used four phase clock pulses and these clocks are at 90° phase lag with each other. The sizes of nmos transistors are W/L=135nm/90nm except bootstrapping nmos devices. For bootstrapping nmos we have used W/L=1215nm/90nm.

The simulation waveforms shown in Fig. 3(b) show the function of 4-bit ripple carry adder in which carry from one stage should propagate to the another stage. Sum of each full adder and output carry is shown in Fig. 3(b).

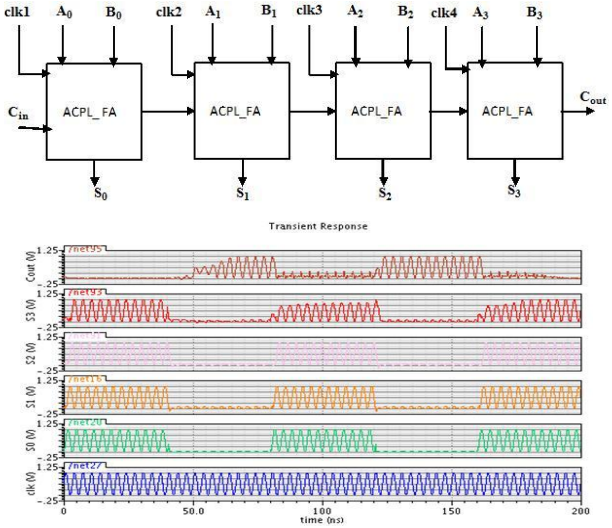


Fig. 3 (a) Schematic of adiabatic CPL 4-bit ripple carry adder

(b) Simulated waveforms for adiabatic CPL 4-bit ripple carry adder

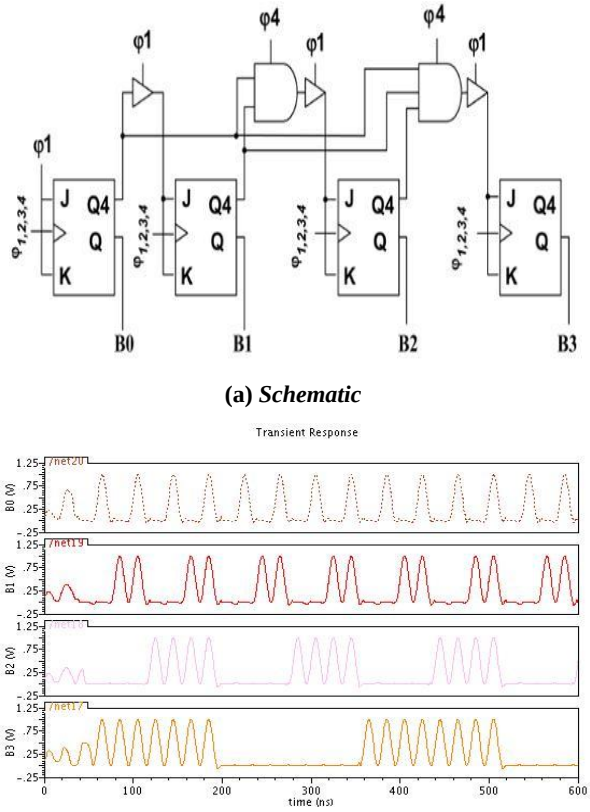
3.2 4-BIT BINARY COUNTER

The schematic of 4-bit binary counter is shown in Fig. 4 (a). For the implementation of binary counter, we have used the sizes of all the gates [8] and flip flops as equal and in which the sizes of bootstrapping transistor are larger than the size of nmos transistor in single gate. For this, we have used four clock pulses namely 1, 2, 3 and 4. These have 900 phase lag with each other.

The complementary inputs and outputs have been excluded for simplicity. This counter uses two AND/NAND logic gates inserted in between the four JK-flip flops. For synchronization purposes, the output signals Q4 and Q4B from the buffer chain inside the JK-flip flop are used as inputs to the AND/NAND gate. Also, an additional buffer is inserted after every AND/NAND gate to synchronize the input signals for the next block.

In this, the input signal is similar to the power clock and output counts the binary clock pulses, ie B0 counts one clock per cycle, B1 counts two clocks per cycle, B2 counts four clocks per cycle and B3 counts eight clocks per cycle .

The simulation waveform of 4-bit binary counter at 100MHz frequency is shown in Fig. 4(b). These waveforms show the complete operation of binary counter.



(a) *Schematic*

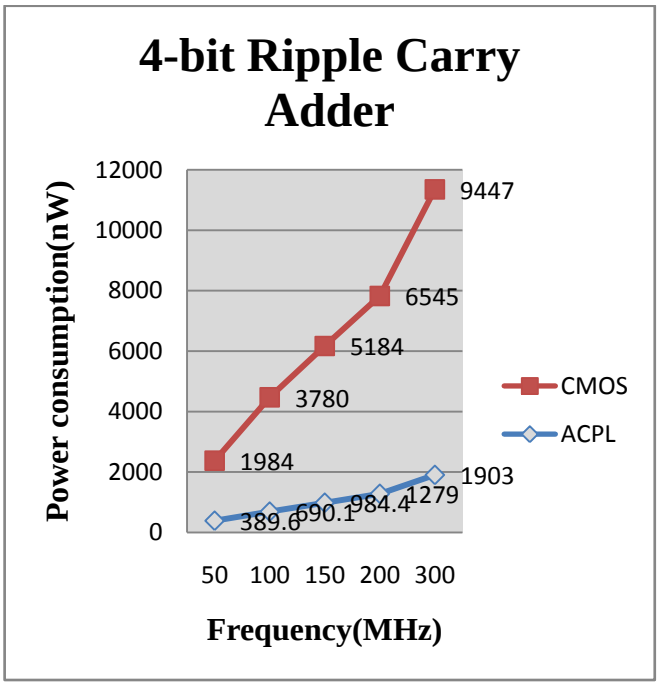
(b) Simulated waveforms for adiabatic CPL 4-bit binary counter

Fig. 4 (a) Schematic of adiabatic CPL 4-bit binary counter

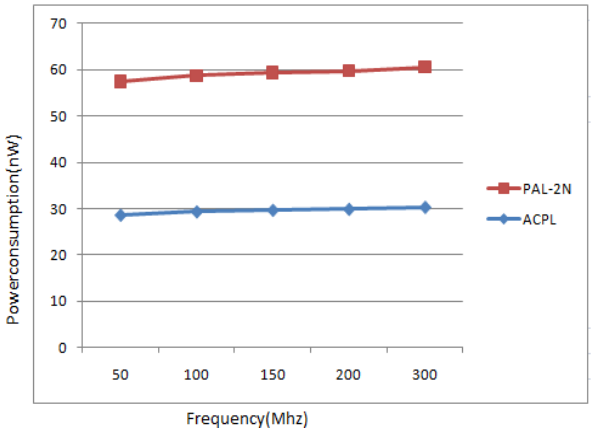
4. SIMULATION RESULTS AND ITS COMPARISONS

The combinational and sequential circuits are simulated using CADENCE design tool based on 90nm technology. The sinusoidal power clocks are 1V peak-to-peak, with 0.5V dc offset.

The power consumed by these circuits at various frequencies ranging from 50MHz to 300MHz is plotted as shown in Fig. 5. For comparison purpose, adiabatic CPL circuits have been simulated with other two adiabatic logics namely static CMOS and PAL-2N. Simulation results show that adiabatic CPL circuits achieves power savings of 81% with CPAL, 88% with 2N-2N2P logic and JK flip-flop achieves 13% to 68% with CPAL, 69% to 91% with 2N-2N2P logic for clock frequencies from 50MHz to 300MHz.



(a) 4-bit ripple carry adder



(b) 4-bit binary counter

Fig.5 Comparison of power consumption versus operating frequency among adiabatic CPL, static CMOS and PAL-2N

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